VILNIUS GEDIMINAS TECHNICAL UNIVERSITY

Agata ROMANOVA

DESIGN OF TRANSIMPEDANCE AMPLIFIERS FOR BROADBAND TIME-DOMAIN OPTICAL REFLECTOMETER SYSTEMS

DOCTORAL DISSERTATION

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Scientific supervisor

Assoc. Prof. Dr Vaidotas BARZDĖNAS (Vilnius Gediminas Technical University, Electrical and Electronic Engineering – T 001).

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The dissertation will be defended at the public meeting of the Dissertation Defense Council of Electrical and Electronic Engineering in the Senate Hall of Vilnius Gediminas Technical University at **10 a. m. on 3 June 2022**.

Address: Saulėtekio al. 11, LT-10223 Vilnius, Lithuania.
Tel. +370 5 274 4956; fax +370 5 270 0112; e-mail: doktor@vilniustech.lt

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agata.romanova@vilniustech.lt

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Agata ROMANOVA

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doc. dr. Vaidotas BARZDĖNAS (Vilniaus Gedimino technikos universitetas, elektros ir elektronikos inžinerija – T 001).

Vilniaus Gedimino technikos universiteto Elektros ir elektronikos inžinerijos mokslo krypties disertacijos gynimo taryba:

Pirmininkas

prof. dr. Algirdas BAŠKYS (Vilniaus Gedimino technikos universitetas, elektros ir elektronikos inžinerija – T 001).

Nariai:

dr. Mindaugas LUKOŠIUS (Inovatyvios mikroelektronikos Leibnico tyrimų institutas, Vokietija, fizika – N 002),

prof. dr. Šarūnas PAULIKAS (Vilniaus Gedimino technikos universitetas, elektros ir elektronikos inžinerija – T 001),

prof. dr. Vytautas URBANAVIČIUS (Vilniaus Gedimino technikos universitetas, elektros ir elektronikos inžinerija – T 001),

prof. dr. Algimantas VALINEVIČIUS (Kauno technologijos universitetas, elektros ir elektronikos inžinerija – T 001).

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Adresas: Saulėtekio al. 11, LT-10223 Vilnius, Lietuva.
Tel.: (8 5) 274 4956; faksas (8 5) 270 0112; el. paštas: doktor@vilniustech.lt

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Abstract

The tremendous growth of Internet traffic in recent years had led to the rapid development of broadband optical communication systems. This rapid growth also increases a demand for the equipment for network deployment, monitoring and repair. One of the typically used instruments is based on a technique known as Optical Time-Domain Reflectometry - OTDR. These instruments are used for characterization and fault detection in optical fibers is based on the analysis of the reflections in time domain.

The research object of the doctoral dissertation is the design and analysis of an programmable-gain CMOS TIA suitable for modern OTDR applications. In order to compare quantitatively different TIA architectures as well as designs produced using different technologies, the work suggests a quantitative measure - Figure-of-Merit (FOM). After evaluating advantages of different TIA types, the dissertation suggests a novel programmable-gain capacitive feedback TIA architecture with PMOS transistor-based biasing circuit for source follower which allows to implement a low-noise broadband TIA. Based on the suggested architecture and using 0.18 μm CMOS and 0.25 μm BiCMOS technologies, TIAs were designed with 1.0 GHz and 0.9 GHz bandwidths accordingly, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ discretely adjustable gains, 1.8 and 1.6 pA/$\sqrt{\text{Hz}}$ noise current spectral densities, 21 mW and 29 mW power consumption at correspondingly 1.8 V and 2.5 V supply voltages and their major characteristics were investigated.

The dissertation consists of an introduction, three chapters, general conclusions, a list of references, the author's publications on the topic of the dissertation and two appendices. The first chapter presents modern TIA architectures, their main parameters, proposed FOM measure and the OTDR requirements for front-end TIAs. The second chapter presents an analysis of the proposed TIA architecture and mathematical models for the transimpedance gain and input-referred noise current spectral density. The third chapter discusses the designed topologies for the proposed TIA architectures and compares the results of the computer simulation with those from the analytical models. The research results of this dissertation are summerized in general conclusions and a comprehensive bibliography with a list of the author's seven publications on the topic of the dissertation are provided.

The results of the dissertation were reported in 7 scientific publications: 3 of them are published in scientific journals referenced in *Clarivate Analytics Web of Science* database with 2 of them having citation index, 2publications in proceedings of international conferences included in *Clarivate Analytics Proceedings* database and 2 publications in conference proceedings included in other international databases. The results of the dissertation research were presented in 5 scientific conferences in Lithuania and abroad.

Reziumė

Pastaraisiais metais sparčiai didėjantis interneto duomenų perdavimo srautas lėmė sparčią plačiajuosčio šviesolaidinio ryšio sistemų plėtrą. Tokia sparti plėtra didina ir tinklo įrengimo, stebėjimo, priežiūros ir gedimų analizės įrangos poreikį. Vienas iš dažniausiai naudojamų šviesolaidinės linijos kokybės detekcijos prietaisų yra laiko srities optinis reflektometras (angl. *optical time-domain reflectometer*, OTDR). Šis prietaisas naudojamas nustatyti ir apibūdinti šviesolaidinių linijų gedimus, analizuojant atspindžius laiko srityje.

Daktaro disertacijos tyrimo objektas yra submikroninių KMOP ir BiKMOP gamybos technologijų pereinamosios varžos stiprintuvų (PVS) architektūros bei jų integriniai grandynai, tinkami šiuolaikinėms OTDR sistemoms kurti. Siekiant kiekybiškai palyginti skirtingų gamybos technologijų ir įvairias PVS architektūras, šiame darbe siūloma kokybės funkcija (angl. *figure of merit*, FOM), apimanti pagrindinius PVS parametrus. Nustačius PVS architektūrų privalumus, disertacijoje siūloma originali, diskretiniu žingsniu valdomo stiprinimo talpinio grįžtamojo ryšio PVS architektūra, leidžianti įgyvendinti ypač plačią praleidžiamų dažnių juostą ir mažus triukšmus. Taip pat remiantis siūloma architektūra ir taikant 0,18 µm KMOP ir 0,25 µm BiKMOP procesų technologijas, suprojektuoti PVS bei ištirti jų pagrindiniai parametrai. Pasiekti PVS parametrai yra 1,0 GHz ir 0,9 GHz praleidžiamų dažnių juosta, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ žingsniu valdomas stiprinimas, 1,8 pA/$\sqrt{\text{Hz}}$ ir 1,6 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinis tankis bei 21 mW ir 29 mW vartojamoji galia, esant 1,8 V ir 2,5 V maitinimo įtampai.

Disertaciją sudaro įvadas, trys skyriai, bendrosios išvados, naudotos literatūros ir autoriaus publikacijų disertacijos tema sąrašas bei du priedai. Pirmajame skyriuje pateikiamos šiuolaikinės PVS architektūros, jų pagrindiniai parametrai, siūloma kokybės funkcija ir reikalavimai OTDR sistemoms. Antrajame skyriuje pateikiama siūlomos PVS architektūros analizė ir matematiniai stiprinimo koeficiento bei srovės triukšmo spektrinio tankio modeliai. Trečiajame skyriuje pateikiami siūlomos PVS architektūros integrinių grandynų topologijų projektavimo ir kompiuterinio modeliavimo rezultatai bei gautų parametrų palyginimas su siūlomais matematiniais modeliais. Šios disertacijos tyrimus apibendrina bendrosios išvados ir pateikiamas literatūros sąrašas bei 7 autoriaus publikacijų sąrašas disertacijos tema.

Disertacijos tema yra atspausdinti 7 moksliniai straipsniai: 3 yra paskelbti mokslo žurnaluose, įtrauktuose į *Clarivate Analytics Web of Science* duomenų bazę, 2 iš jų su citavimo indeksu, 2 yra paskelbti tarptautinių konferencijų medžiagose, įtrauktose į *Clarivate Analytics Proceedings* duomenų bazę, bei 2 yra paskelbti mokslo konferencijų medžiagose, referuojamose kitose tarptautinėse duomenų bazėse. Disertacijoje atliktų tyrimų rezultatai buvo pristatyti 5 mokslinėse konferencijose Lietuvoje ir užsienyje.

Notations

Symbols

A	voltage gain
BW	useful bandwidth
$BW_{-3\mathrm{dB}}$	-3 dB bandwidth
BW_{ENBW}	effective noise bandwidth
Bs	back-scattering coefficient
C_{C}	isolation capacitance
C_{F}	feedback capacitance
C_{O}	output capacitance
C_{i}	capacitance i
C_{ox}	gate oxide capacitance per unit area
C_{T}	total input capacitance
F_{1}	gain of the feedback block
G_{i}	voltage gain of the ith block
G_{Σ}	total voltage gain
$H\left(\mathrm{j}\omega\right)$	transfer function
$H_{\max}$	maximum value of transfer function $H\left(\mathrm{j}\omega\right)$

I	current
I_{G}	gate current
I_{dark}	dark current of the photodiode
K_{f}	flicker noise constant
L_{i}	inductance i
L_{Mi}	length for the ith transistor channel
M	multiplication factor of avalanche phododiode
M_{i}	transistor i
Q	quality factor
P	power
P_0	pulse power
P_{NEP}	noise equivalent power
P_{bsc}	power of back-scattered light
P_{refl}	reflected power
R_{F}	feedback resistance
R_{IN}	mid-frequency approximation of input impedance
R_{L}	reflection coefficent
R_{T}	mid-frequency approximation of Z_{T}
R_{i}	resistance i
S	maximum signal level at the output
T	absolute temperature
V	voltage
V_{DD}	supply voltage
V_{gs}	gate-source voltage
V_{th}	threshold voltage
W_{Mi}	width for the ith transistor channel
X	reactance
Z	impedance
Z_{IN}	input impedance
Z_{T}	transimpedance of amplifier
c	speed of light in vacuum
f	frequency (ordinary)
f_0	frequency (ordinary) of the output pole
f_{c}	cutoff frequency
f_{C}	corner frequency of flicker noise
f_{T}	technology transit frequency
g_0	channel conductor at zero drain-source voltage
g_{m}	total transconductance

g_{ds}	total conductance
$g_{\mathrm{m,i}}$	transconductance of ith transistor
$g_{\mathrm{ds,i}}$	conductance of ith transistor
$i_{\mathrm{n,PD}}$	photodiode's noise current
$i_{\mathrm{n,TIA}}$	amplifier input-referred noise current
$i_{\mathrm{n,i}}$	noise current of ith component
i_{PD}	photodiode's current
i_{tot}	total input noise current
$\overline{i_k^2}/\Delta f$	spectral density kth noise current component squared
j	imaginary unit
$\mathrm{k_B}$	Boltzmann constant
n	refractive index
q	electron charge
r	reflection amplitude
r_{DSi}	efficient resistance of ith transistor
s	complex variable $s = \mathrm{j}\omega$
t	time
v	speed of light in medium
$v_{\mathrm{n,TIA}}$	amplifier input-referred noise voltage
$\Delta\tau_{\mathrm{g}}$	group delay variation
γ	excess noise coefficient
λ	wavelength
μ	charge-carrier effective mobility
ϕ	phase
τ	time constant
τ_{g}	group delay
ω	angular frequency
ω_0	angular frequency of the output pole
ζ	damping factor

Abbreviations

ADC	Analog-to-Digital Converter
ADZ	Attenuation Dead Zone
AGC	Automatic Gain Control
APD	Avalanche Photodiode
ASIC	Application-Specific Integrated Circuit
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BIT	Built-In Test

BJT	Bipolar Junction Transistor
CG	Common-Gate
CMOS	Complementary Metal Oxide Semiconductor
CR-OTDR	Correlation-Based Optical Time-Domain Reflectometry
CS	Common-Source
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
EDFA	Erbium-Doped Fiber Amplifier
ESD	Electrostatic Discharge
FBG	Fiber Bragg Grating
FOM	Figure-Of-Merit
FVF	Flipped Voltage Follower
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
InP	Indium Phosphide
IoT	Internet-of-Things
ISI	Intersymbol Interference
LIDAR	Light Detection and Ranging
LNA	Low-Noise Amplifier
MA	Main Amplifier
MEMS	Microelectromechanical Systems
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
NMOS	N-Channel Metal-Oxide-Semiconductor
OTDR	Optical Time-Domain Reflectometry
PD	Photodetector
PIP	π-type Inductor Peaking
PMOS	P-Channel Metal-Oxide-Semiconductor
PON	Passive Optical Networks
PSD	Power Spectral Density
RGC	Regulated Cascode
RMS	Root-Mean Square
SFB	Shunt Feedback
SiGe	Silicium Germanium
SNR	Signal-to-Noise Ratio
SOC	System-on-Chip
STI	Shallow-Trench-Isolation
TIA	Transimpedance Amplifier

Contents

[1]The annexes are supplied in the enclosed compact disc.

Introduction

Problem Formulation

Optical communication networks form the backbone of modern Internet. Fiber optic technology is often considered to be the most important foundation for the development of future network infrastructure as it provides extremely high bandwidth (theoretically up to 50 Tb/s), low signal distortion and requires low power with reduced space requirements, low material consumption and is relatively low-cost (Lee & Mukherjee, 2004). The exponential growth of Internet traffic as well as constantly increasing number of new services and functions available online are driving both the development of new networking technologies and capacity ramp-up of existing infrastructure. Such rapid development of optical communication systems also results in the increasing need for network installation, monitoring, maintenance, and fault analysis equipment. One of the most commonly used equipment for optical line quality assessment is a so-called optical time-domain reflectometer (OTDR). The operation principle of this device is based on Rayleigh scattering of light in a fiber, where an optical pulse is injected using a laser. As the optical pulse propagates along the fiber, light interacts with the defects in the material of the fiber and part of the light is reflected back causing the reflection signal to be detected at the injection side. An optical receiver consisting of a photodetector and a transimpedance amplifier (TIA) converts the reflected light signal into a

current pulse and integrates it to obtain an amplified voltage signal, which is then sampled and digitally processed. The basic parameters of the reflectometer (dynamic range and dead zone) are often limited by the performance of the front-end TIA. As TIA forms the first step in optical signal processing, its gain, noise levels, bandwidth and other parameters may strongly limit the overall sensitivity of the instrument. Typically in modern OTDR systems the front-end TIAs are implemented from discrete components that result in high parasitics and noises, increased power consumption, narrow bandwidth, and low potential for optimization and performance improvement. It shall be also noted that most of these amplifiers are based on classical resistive feedback TIA architectures which are also characterized by higher noise levels and reduced bandwidth. Therefore, the dissertation analyzes the problem of selecting the TIA architecture which fits the best the requirements of modern OTDR systems and their implementation on a single chip using modern sub-micron CMOS and BiCMOS technologies. At the same time, both qualitative and quantitative analysis shall be performed while choosing a proper TIA architecture and corresponding mathematical models shall be developed which describe the behavior of the amplifier over a wide frequency range. Therefore, in order to improve the performance of next generation OTDR instruments it is necessary to look for new TIA architectures and design integrated circuits based on them. Thus, the problem addressed in this dissertation is the selection of TIA architecture that best meets the requirements of modern OTDR systems and implementation of this architecture as an integrated circuit using modern submicron CMOS and BiCMOS technologies. While choosing the TIA architecture and designing the circuit, both qualitative and quantitative analysis shall be performed and accurate mathematical models, describing the main parameters of the circuit, shall be developed. To solve the problem, a working hypothesis is put forward and it was proved that capacitive feedback TIA architecture enables the creation of programmable-gain, broadband, low-noise TIA integrated circuits using modern commercially available submicron CMOS and BiCMOS manufacturing technologies.

Relevance of the Thesis

Although in the last decade of the 20th century the major part of the semiconductor industry growth was driven by personal computers, an important change took place around the year 2000, when the semiconductor revenue from the communications sector exceeded those from the computer sector (Buss, 2002). It is also clear that this growth continues to this day as demand for the Internet-of-Things (IoT), cloud, data and storage services continues to grow. For example, from the year 2000 till now the number of internet users in the world has grown more than 10.6 times to 5.07 billion (STATISTA, 2022). Such rapid growth in number of the

users had lead to growth in Internet traffic and correspondingly leads to an increase in the usage of the fiber-optic infrastructure. Here the fiber-optic systems currently form the backbone of the world's communications infrastructure, accounting for the majority (more than 99%) of global data traffic (CORDIS, 2022). However, such constant exponential growth of the data traffic is also placing constantly increasing requirements on the properties of the optical communication channel, its quality and reliability. Optical line testing is typically based on the methods of optical reflectometry, where OTDR instruments measure all the parameters of the optical fiber relevant for proper operation of communication channel. Due to a relatively small size of the OTDR market, the TIAs typically used in the instruments have been manufactured using mostly discrete components. This results in the TIAs having relatively narrow bandwidth often below 100 MHz (Charlamov, 2013; Charlamov & Navickas, 2015), while modern CMOS-based optical receivers for communication systems easily reach tens of GHz bandwidth. Such circuits have high parasitic capacitances, higher power consumption, higher noises and it may be hard to achieve a large dynamic range with good signal-to-noise ratio (Yeom et al., 2019). Most of these problems can be if not eliminated, then significantly mitigated by implementing the front-end TIA as an integrated circuit. Such solutions may significantly improve the performance of the OTDR equipment due to increased bandwidth and reduce the instrument's dead zone compared to solutions using either discrete components of suboptimal configuration or commercial general-purpose TIAs. Additionally, the integrated circuit implementation can be designed to match exactly the specification of the OTDR instrument, which in turn is difficult to implement with existing commercial TIA products. It should be also noted that the relatively expensive GaAs, InP, HBT and HEMT have been historically used to design and manufacture broadband and low-noise TIAs for higher performance applications. Therefore, in order to reduce the cost and increase the competitiveness of the developed OTDR instruments, one is considering more often the financially attractive modern submicron CMOS and BiCMOS technologies with f_{T} in the range of several tens of GHz.

In Lithuania, research related to TIA circuits is not widespread. The results of the research on this topic are published by VILNIUS TECH researchers J. Charlamov and R. Navickas (Charlamov & Navickas, 2015). Researchers K. Kiela, M. Jurgo, A. Vasjanov, V. Macaitis, L. Kladovščikov and the private companies Lime Microsystems (Vilnius) and Si Femto (Kaunas) are also conducting research in the field of wireless communication and high-speed integrated circuits. In summary, it can be stated that modern TIAs have not been sufficiently researched and described. The research carried out in the dissertation is relevant and the obtained results along with further research will accelerate the development of next-generation OTDR instruments.

The Object of the Research

The research object of the dissertation - transimpedance amplifier (TIA) architectures and their implementations as integrated circuits in modern CMOS and BiCMOS.

The Aim of the Thesis

The aim of the dissertation is to develop and implement programmable-gain wideband low-noise TIAs for front-ends of optical time-domain reflectometers using submicron CMOS and BiCMOS integrated circuits manufacturing technologies.

The Objectives of the Thesis

To achieve the aim of the thesis, the following objectives were formulated:

1. To carry out research on the latest reported TIA architectures by presenting results of both qualitative and quantitative analysis. Examine the suitability of these architectures for the development of the front-end TIA to be used in modern time-domain optical reflectometers.
2. To develop a novel capacitive feedback programmable-gain TIA architecture with associated gain and noise mathematical models which will enable development of broadband ($\geq$1 GHz) low-noise ($\leq$5.0 pA/$\sqrt{\text{Hz}}$) TIAs.
3. To design and investigate the performance of TIA integrated circuits by implementing the proposed architecture using modern 0.18 μm CMOS and 0.25 μm BiCMOS manufacturing processes.

Research Methodology

Analytical, mathematical and computer simulation methods have been employed for the design and investigation of capacitive feedback TIAs. Analytical methods were applied in generalizing different TIA architectures, where mathematical and computer simulation methods were employed to design the performance analysis of the integrated circuits with capacitive feedback TIAs. The production technology libraries for TSMC 0.18 μm CMOS and IHP 0.25 μm BiCMOS were used for design of the TIA integrated circuits. The modeling and analysis of the designed circuits was conducted using Cadence Virtuoso software package for professional integrated circuit design.

Scientific Novelty of the Thesis

The following new and significant results for electrical and electronic engineering were obtained during the preparation of the dissertation:

1. A new FOM metric was proposed to enable a quantitative comparison of TIA of different architectures and produced with different technological processes. The newly proposed FOM is based on the main TIA parameters such as transimpedance gain, bandwidth, total input capacitance, power consumption, and noise current density.
2. A novel capacitive feedback TIA architecture with PMOS transistor-based biasing circuit was proposed featuring low noise (1.8 pA/$\sqrt{\text{Hz}}$), wide bandwidth (1 GHz) and supporting programmable-gain realization. The proposed design can be fabricated using modern submicron CMOS and BiCMOS manufacturing technologies.
3. New and more accurate mathematical models for transimpedance gain and noise current density in capacitive feedback TIA were proposed. The models extend the accuracy for circuit parameter modeling in the frequency range up to 1 GHz compared to the previously published works of other authors and whose discrepancy with computer simulation results does not exceed: 5% for the transimpedance gain in the frequencies up to 1 GHz; 15% in input-referred noise current spectral density at 500 MHz and Z_T = 10 kΩ.
4. Using modern submicron 0.18 μm CMOS and 0.25 μm BiCMOS manufacturing technologies, programmable-gain capacitive feedback TIAs were designed with 1 GHz / 0.9 GHz bandwidth, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ step-programmable gains, 1.8/1.6 pA/$\sqrt{\text{Hz}}$ input-referred noise current spectral density and 1.8 V / 2.5 V supply voltage and their performance was investigated.

Practical Value of the Research Findings

The results obtained in this dissertation were used in the design of TIA integrated circuits using modern submicron 0,18 μm CMOS ir 0,25 μm BiCMOS technologies. Suggested quantitative performance indicator FOM can be used for comparative analysis and evaluation of different TIA architectures and manufacturing technologies, while new step programmable-gain concept for capacitive feedback TIA together with corresponding mathematical models can be used for developing new optical time-domain reflectometry instruments. The results obtained from the research can be also applied for other optical systems, where the problem of

low noise, high sensitivity and wideband is of a particular importance, and can be employed for further research and improvement of TIA-based optical or related systems.

The Defended Statements

The following defended statements have been formulated during the work on dissertation:

1. A new quantitative performance FOM was proposed which can be used for a comparative analysis of different TIA architectures and their implementations with different CMOS and BiCMOS technologies and which mathematically emphasizes the importance of a proper trade-off between the gain-bandwidth product and the input-referred noise current spectral density for modern time-domain optical reflectometer systems.
2. The proposed mathematical models for the transimpedance gain and input-referred noise current density extend the accuracy for circuit parameter modeling in the frequency range up to 1 GHz with the discrepancy to the computer simulation results as follows: 5% for the transimpedance gain when measured in the frequency range up to 1 GHz; 15% for noise current spectral density at 500 MHz and gain Z_T = 10 kΩ.
3. CMOS TIA designed using the proposed architecture ensures 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ programmable gain values, 1 GHz bandwidth and 1.8 pA/$\sqrt{\text{Hz}}$ input-referred noise current density at the base gain of 10 kΩ with 21 mW power consumption at 1.8 V power supply.
4. Suggested capacitive feedback TIA with discrete gain control mechanism can be implemented in commercially available submicron TSMC 0.18 μm CMOS and IHP 0.25 μm BiCMOS technologies.

Approval of the Research Findings

The results of the research were published in seven scientific publications: two publications (Romanova & Barzdenas, 2019a; Romanova & Barzdenas, 2021a) in scientific journals referenced in *Clarivate Analytics Web of Science* database and having citation index; one publication (Romanova & Barzdenas, 2020a) in scientific journal referenced in *Clarivate Analytics Web of Science* database, but having no citation index; two publications in conference proceedings included in *Clarivate Analytics Web of Science „Conference Proceedings“* database (Romanova & Barzdenas, 2018; Romanova & Barzdenas, 2020c); and two publications (Romanova &

Barzdenas, 2019b; Romanova & Barzdenas, 2020b) in conference proceedings included in other international databases.

The results of the research conducted in the dissertation have been published in five scientific conferences in Lithuania and abroad:

- 21st Conference for Young Researchers "Science – future of Lithuania". Vilnius, Lithuania, 16 March 2018;
- 2018 Open Conference of Electrical, Electronic and Information Sciences (eStream), Vilnius, Lithuania, 26 April, 2018;
- 2019 IEEE Microwave Theory and Techniques in Wireless Communications (MTTW), Riga, Latvia, 1-2 October, 2019;
- 2020 IEEE Open Conference of Electrical, Electronic and Information Sciences (eStream), Vilnius, Lithuania, 30 April, 2020;
- 2020 27th International Conference on Mixed Design of Integrated Circuits and Systems, MIXDES 2020, Wroclaw, Poland, 25-27 June, 2020.

Structure of the Dissertation

The dissertation includes an introduction, three chapters, general conclusions, list of references and a list of seven publications by the author on the topic of the dissertation. The volume of the dissertation is 184 pages, in which 133 indexed equations, 73 figures and 6 tables are presented. The dissertation is based on 115 works of other authors.

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1

Analysis of Modern Transimpedance Amplifier Architectures and Applicability to OTDR Systems

In this chapter, several different designs for low-noise TIA are presented and discussed. A comparison of the main performance characteristics of the approaches is provided based on the available literature in order to support the choice of the best-suited design for the target OTDR application. The basic principles behind the OTDR technique are also explained.

The research results, presented in this chapter, have been already partially demonstrated at the international "eStream" scientific conference (Romanova & Barzdenas, 2018) and published in (Romanova & Barzdenas, 2019a) paper.

1.1. TIA Architectures and Application Areas

1.1.1. Application Areas and CMOS Challenges

It was during the late 1960s and early 1970s when TIAs found widespread usage in optical coupling and optical communication receivers (Razavi, 2019) even though the underlying concepts behind TIAs are as old the concept of the feedback amplifier itself. TIAs are typically used in applications where weak signals from

current-mode sensors (e.g. from a diode or, in general, from any sensor with current output) have to be converted to the output voltage of the amplitude sufficient for subsequent amplification, signal processing and analysis. The popularity of the TIA in optical communication is due to the fact that the PD can be effectively modeled as a current source. Apart from being used in optical communications such as families of 2.5, 10, 25 or 40 Gb/s systems (Shahdoost et al., 2014), the TIA are also widely adopted in readout circuits of MEMS sensors (Keshri, 2010; Mekky et al., 2013; Royo et al., 2017; Salvia et al., 2009; Woo et al., 2017), LIDAR (Ma et al., 2018), miniaturized magnetic resonance systems (Ghanad & Dehollain, 2016), acustic wave imaging (Li et al., 2006), bio-sensors (Hu et al., 2010a; Wilson, 2014; Wilson & Chen, 2014) as well as biological applications (Kamrani et al., 2013), ultrasound imaging (Cenkeramaddi & Ytterdal, 2009; Monsurro et al., 2010), spectroscopy (Chaddad & Tanougast, 2014; Rajabzadeh et al., 2018), etc. Obviously, this broad range of applications had resulted in different sets of constraints when it comes to choosing an amplifier design and topology. Although optical communication systems have pushed the requirements for the amplifiers towards higher gain-bandwidth products, the requirements for lower-noise and reduced power consumption may become prevalent for designs targeting implantable sensors while staying in a much lower frequency range (Shahdoost et al., 2014).

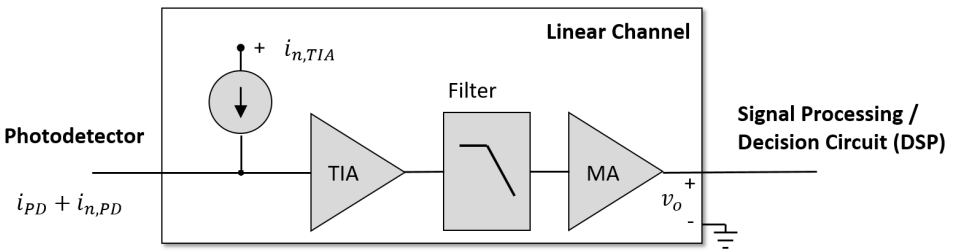

Fig. 1.1. The context and the structure of the linear channel

The TIA can be considered as the first part (the other two are the filter and MA) of a so-called linear channel for the input current processing (see Fig. 1.1). The linear channel is modeled as a block of a complex frequency response that relates the amplitude and the phase of the output voltage to those of the input current. The modeling of the linear channel as a product of three responses is shown here more for the logical separation and often, in practice, the filter stage or the MA can be omitted or integrated into the TIA. In practical receiver design the TIA may also incorporate an AGC to accommodate a wide range of input currents and to work under input overload conditions (Jia Xu & Zhenghao Lu, 2011; Mekky et al., 2013; Razavi, 2002). As an input to the linear channel a current i_{PD} from a PD with its noise current $i_{\mathrm{n,PD}}$ is shown, although any current sensing device can

be used within a broader sensing context. The front-end preamplifier (i.e. the TIA) is the most critical component affecting some of the most important characteristics of the optical receiver such as the noise sensitivity and the speed of a complete system (Oh & Park, 2007; Park et al., 2007; Royo et al., 2016).

At the output of the linear channel, voltage is formed which can be later used by either the signal processing or decision circuits. For the discussion, one assumes that the PD's (of any type) itself is not a limiting factor for the front-end performance and we put the focus of the discussion on the characteristics of the TIA itself. Still, different detectors have varying primary noise mechanisms which have to be considered when performing circuit-level simulations for feasibility analysis of different TIA designs. For example, although shot noise is believed to be the major noise source for detector, avalanche noise with the excess noise factor has to be considered if the APD detector type is used. Typically, it is also assumed that the PD is sufficiently linear so that signal distortions are minimized. The noise characteristics of the linear channel are modeled as a single equivalent noise current generator $i_{\mathrm{n,TIA}}$ at the channel's input. This noise current source is not white, but stationary, and its amplitude distribution can be often well approximated by a Gaussian. This is quite opposite for the statistics of a simple PD, which is often assumed to have white, but non-stationary noise.

High-speed TIAs have been traditionally implemented using single-ended topologies due to their relative simplicity, lower power consumption, smaller die area and better noise performance. However, at high frequencies, single-ended topologies may become susceptible to supply noise and may be plagued with stability problems stemming from parasitic feedback paths (Mohan et al., 2000; Tao & Berroth, 2003). Thus, due to practical considerations, one often ends up with more robust differential designs which ensure good common-mode rejection, especially when one considers practical circuits where the ultimate goal is the tight integration of the analog and digital functions on a single chip (Atef & Zimmermann, 2012; Tao & Berroth, 2003).

Historically, higher performance and low-noise TIAs have been developed using non-CMOS high f_{T} technologies such as GaAs, InP, HEMT, HBT and SiGe BiCMOS (Bertenburg et al., 1996). Although those technologies have been chosen due to their excellent noise, bandwidth and gain performance (Liu et al., 2012; Mohan et al., 2000), standard CMOS is gaining popularity due to its advantages both in cost and in the inherent support for higher integration (Atef & Zimmermann, 2012; Razavi, 2002; Yong-Hun Oh & Sang-Gug Lee, 2004). One can also consider optical transceivers to employ hybrid components integrating e.g. III-V devices with CMOS circuits, but that can result in variable parasitics on the interfaces and should be carefully evaluated (Yiling Zhang et al., 2008).

On the other hand, what relates to classical CMOS, the number of transistors in the microprocessor doubles every 18 and later 24 months, while the price of a

transistor decreased exponentially over the last decades (Moore, 2003, 2006). Here the steady down-scaling of the transistor dimensions over the past four decades was the major stimulus to the growth of the semiconductor industry and its acceptance as the basis for blooming IT infrastructure (Taur, 2002). This support for efficient down-scaling is an important feature while selecting the technology for the design as it enables the performance-enhancing functionality including complex biasing circuits, advanced ESD designs etc., something which may be not commercially feasible in designs with available III-V technologies (Razavi, 2002)[1]. Of course, when having the data processing and the interface chips with different technologies, the packaging costs may increase while the overall system performance may decrease due to interconnecting bond wires and pads (Szilagyi et al., 2014). CMOS processes can also afford structures that have been originally used in III-V technologies for microwave and millimeter-wave applications and this well-known advantage of III-V technologies is not relevant anymore when choosing against standard commercial CMOS. Previously, some OTDR products have been also developed using the BJT process. However, BJT is a current-controlled device as the output characteristics of the BJT depend on the base current. As a result, BJT has a large current when compared to the CMOS-based approach with relatively large power consumption. Here standard CMOS also brings advantages in power consumption which may be critically important both for portable devices and promising BIT applications. Finally, there is also a large production capacity available from the foundries and one does not need to owe a custom line in order to keep up with the trends in the market (Zampardi, 2010).

Although CMOS technology is an excellent candidate when one aims for the design of a truly low-cost and low-power amplifier, there are significant technical challenges that make the CMOS-based development path more than non-trivial. First of all, the continuous down-scaling of the supply voltage is not automatically advantageous for analog integrated circuits as it imposes many challenges in the design of higher performance integrated circuits (Buss, 2002; Cenkeramaddi & Ytterdal, 2009) with additional issues caused by the gate currents (Annema et al., 2004)[2]. Other limitations include poor matching of small components, high $1/f$ noise and often an absence of on-chip passive components with adequate analog characteristics (Buss, 2002). Further technical challenges are related to the contradicting requirements of a typical TIA such as high and accurate transimpedance gain, adequate bandwidth, good closed-loop stability and, at the same time, low input noise and low or moderate power consumption.

[1] Even though this argument may be less relevant for lower complexity circuits such as TIA itself, it may become critical when a full receiver or even complete OTDR circuit shall be integrated in a single chip.

[2] According to (Annema et al., 2004), analog circuits can benefit from scaling CMOS technologies only if the supply voltages are not scaled unlike in digital counterparts.

A special challenge while considering design in CMOS is due to inferior parasitic capacitances in a MOS transistor (Chao-Yung Wang et al., 2007; Escid et al., 2013; Jin & Hsu, 2006) and its poor device-level performance of such as small transconductance (Yong-Hun Oh & Sang-Gug Lee, 2004) and high noise (Wu et al., 2005) which make the broadband design a non-trivial task (Han et al., 2010). Although scaling of the CMOS process to nanometer range enables the design of high-speed and low-cost analog circuits, the corresponding scaling of the supply voltage in nanometer CMOS restricts the design possibilities such as stacking of the circuits (Abd-elrahman et al., 2016). As a result, one often ends up in cascaded stages for amplifiers with high gain-bandwidth products which also consume more power. Moreover, the stability of such designs is often worse when compared to simpler single-stage solutions (Abd-elrahman et al., 2015, 2016). Thus, adoption of modern CMOS for higher performance analog design may also need a revision of widely adopted architectures to take an advantage of low-voltage and low-cost digital logic (Buss, 2002).

The straightforward means of increasing the gain usually result in increased chances of instability, while the requirement for lower noise performance often translates into higher power consumption. Although the reduction of IC channel width does not shrink the size of the analog ICs at the same rate as that of digital ones, such scaling significantly increases the costs of production. Therefore, one may be not interested to use the most advanced and expensive CMOS technology and 0.18 μm and 0.25 μm technologies were selected for the presented design. Still, III-V technologies are continuously becoming feature-rich and with the addition of field-effect transistors to most HBT processes they start to provide the designers higher flexibility in implementing circuits for more advanced and specific applications (Zampardi, 2010).

A number of practical issues may also limit the modeling capabilities for CMOS at high speeds. One of the principal difficulties in modeling MOSFETs for optical circuits relates to their thermal and flicker noise. Here the excess noise coefficient γ and the flicker noise corner frequency of short-channel transistors are often obtained by direct device measurements for each technology generation (Razavi, 2002). Thus, a competitive CMOS TIA design shall rely heavily on circuit design techniques to overcome the technology limitations and leverage the functionality that can be implemented.

Several works have attempted to provide a comparative analysis on TIA using different technologies (Praveen et al., 2014; Rashed & Tabbour, 2018). However, such analysis possess certain difficulties due to different topologies and varying nodes so that a clear statement can be hardly made. Even under such conceptual constraints, the authors in (Praveen et al., 2014) claimed that the CMOS-based approach can show better results when compared to similar BiCMOS processes.

1.1.2. Main TIA Parameters

In the section below we will briefly discuss the most important TIA performance measures which will be used later for selecting the most promising design concept for implementing the front-end in low-cost and low-noise OTDR instruments.

A. Gain

The *transimpedance* value $Z_{\mathrm{T}}(s)$ is the first from several performance indicators which is typically used to describe the performance of a TIA. The transimpedance is defined as a ratio of the output voltage $V_{\mathrm{out}}(s)$ over the input current $I_{\mathrm{in}}(s)$ in a linear input signal domain with $s = \mathrm{j}\omega$:

$$Z_{\mathrm{T}}(s) = \frac{V_{\mathrm{out}}(s)}{I_{\mathrm{in}}(s)}. \tag{1.1}$$

For simplicity we may sometimes write Z_{T} without explicitly denoting the s-domain. In practice one may also use the value R_{T} which corresponds to the mid-band value of $|Z_{\mathrm{T}}(s)|$ and is usually called the transresistance. At the end the designer typically wants the transimpedance Z_{T} to be large as possible to relax the gain and the noise requirements for the subsequent amplifier stages. Unfortunately, the wideband bandwidth requirement makes high gain difficult to obtain, since the gain and the bandwidth are strongly related. Since the output buffer (not shown in Fig. 1.1) usually provides a small amount of gain, it is TIA and MA together that determine the overall gain of the system.

B. Bandwidth

This is the second most important parameter which is typically used to characterize the performance of a TIA. The value $BW_{-3\mathrm{dB}}$ is defined as the upper frequency at which Z_{T} drops 3 dB below its mid-band range. Additionally, maximum permitted peaking in frequency response has to be specified along with the original bandwidth, because sometimes one can try to improve the bandwidth at the expense of higher inductive peaking which is not always acceptable depending on the application requirements. Note that amplifiers designed for optical applications usually also have low-frequency cutoff.

C. Noise

This is the third most important TIA parameter which is also called Input-Referred Noise Current (also often referred as Equivalent Input Noise Current) as depicted in Fig. 1.1 and which determines the overall sensitivity of the circuit. Although, in general, both the TIA and the MA have an impact on the noise performance, the TIA plays a key role due to its proximity to the signal source. The same holds

for a cascaded configuration where the noise is dominated by the first stage since the impact of the noise by subsequent stages is reduced through the gain of the previous stages. As it follows from basic noise models, the relative contribution of the noise sources can be only considered with respect to known system bandwidth. Since the PD usually exhibits a high shunt resistance in parallel with the PD capacitance, the input-referred noise current is sufficient to be modeled as a current source. However, the current noise values should be typically quoted together with the PD capacitance which determines the overall source impedance. In practice, the capacitances of the ESD circuit and the input pad must also be specified, since together with the PD capacitance they have a significant influence on both bandwidth and noise performance of the amplifier.

Input-referred noise current spectrum $\overline{i^2_{\mathrm{n,TIA}}(s)}$ is obtained from voltage spectrum $\overline{v^2_{\mathrm{n,TIA}}(s)}$ divided by the transimpedance gain squared (Jin & Hsu, 2008a):

$$\overline{i^2_{\mathrm{n,TIA}}(s)} = \frac{\overline{v^2_{\mathrm{n,TIA}}(s)}}{|Z_{\mathrm{T}}(s)|^2}. \tag{1.2}$$

Input-referred noise current spectrum is measured in $\mathrm{pA}^2/\mathrm{Hz}$ and is often presented as its spectral density, correspondingly $\mathrm{pA}/\sqrt{\mathrm{Hz}}$. The above value has to be calculated for each frequency and therefore cannot be completely characterized by a single number and, in general, a complete PSD needs to be provided for a valid comparison. For simplicity, an average value over the bandwidth is often provided and used to benchmark the designs. This can be interpreted as the noise current density of the white noise that must be applied to the input of a noise-free TIA to reproduce the RMS output noise (but not its spectral distribution) of a real noisy TIA. In addition, the RMS noise current can be calculated as follows (Jin & Hsu, 2008a):

$$i^{\mathrm{rms}}_{\mathrm{n,TIA}} = \frac{v^{\mathrm{rms}}_{\mathrm{n,TIA}}}{R_{\mathrm{T}}} = \frac{1}{R_{\mathrm{T}}}\sqrt{\int_0^{>2BW_{-3\mathrm{dB}}} |Z_{\mathrm{T}}(f)|^2 \cdot \overline{i^2_{\mathrm{n,TIA}}(f)}df}. \tag{1.3}$$

Note in the expression above upper integration bound is set to at least double the bandwidth of the amplifier.

D. Group-Delay Variation

A group-delay τ_{g} is calculated from the phase ϕ as follows:

$$\tau_{\mathrm{g}}(\omega) = -\frac{d\phi}{d\omega}, \tag{1.4}$$

where $\omega = 2\pi f$ is the angular frequency and ϕ is in radians. Thus, a linear phase results in a constant group delay. Then, the group-delay variation $\Delta\tau_{\mathrm{g}}$ is defined as the largest deviation of the computed group delay from the constant group delay approximation within the bandwidth of interest. The $\Delta\tau_{\mathrm{g}}$ becomes an important indicator of the linear distortions in TIA. Note that inductive peaking, which is a popular technique in high-speed circuit design, while being extremely helpful in boosting the bandwidth, may have a detrimental effect on $\Delta\tau_{\mathrm{g}}$ due to the introduction of high-Q complex poles. Unfortunately, this characteristic is often omitted when reporting novel TIA designs.

Although the four measures from above form a typical basis for TIA comparison (even if the group-delay is less often reported), some other performance measures are also highly relevant in practice. For multichannel TIA, a crosstalk between the channels can be also of high relevance. Of course, other constraints such as technology, power consumption (this one is extremely often used for comparison), supply voltage requirements, and chip area are important when evaluating the pros and cons of different designs.

1.2. Modern TIA Architectures

1.2.1. Typical Designs

As mentioned before, the TIA has a decisive role in the overall performance of the optical receiver. It forms the pre-amplifier and plays a similar role within the system as a LNA in wireless applications. We start the discussion with several basic and well-known designs and compare their performance in terms of three main characteristics such as gain, noise, and achievable bandwidth.

The term TIA typically evokes an image of a so-called resistive SFB TIA as shown in Fig. 1.3. However, this well-known topology is just one of the possible realizations of the general current-to-voltage conversion concept which had gained a wide adoption due to its reasonable balance of the most important performance characteristics such as transimpedance gain, bandwidth, and moderate noise levels (Escid et al., 2013). Alternative designs are possible and some of them can be considered to be even better candidates for specific applications.

A. Low- and High-Impedance Front-Ends

The discussion on typical TIA designs can be started with extremely simple circuits such as classical low- and high-impedance front-ends implemented using a termination resistor (Kamrani et al., 2013). These simple circuits act as basic current-to-voltage converters and thus can be considered the simplest and purest form of

TIA (see Fig. 1.2). The transresistance value becomes:

$$R_{\mathrm{T}} = R_{\mathrm{L}}, \tag{1.5}$$

while the bandwidth becomes:

$$BW_{-3\mathrm{dB}} = \frac{1}{2\pi R_{\mathrm{L}} C_{\mathrm{T}}}, \tag{1.6}$$

with $C_{\mathrm{T}} = C_{\mathrm{D}} + C_{\mathrm{IN}}$ and the noise:

$$\overline{i^2_{\mathrm{n,TIA}}} = \frac{4\mathrm{k_B}T}{R_{\mathrm{L}}}, \tag{1.7}$$

where C_{IN} is the input (including gate) capacitance and C_{D} is the sum of all capacitances of the active area of the PD as well as the associated parasitic capacitances such as those arising from the bond-pads, ESD circuits, etc (Park et al., 2007), $\mathrm{k_B}$ is the Boltzmann constant and T stands for the absolute temperature. The expressions above make it clear that the design exhibits a direct trade-off between the bandwidth and the noise for the given input capacitance. Larger bandwidth requires smaller resistance R_{L}, but a small value for the latter results in larger noise to the input. Thus, although a problem with the noise and the gain can be partially resolved by increasing the value of the resistor (a so-called high-impedance configuration), the bandwidth and the dynamic range are then correspondingly reduced. Thus, the structure with high impedance offers higher sensitivity and low noise while suffering from limited dynamic range and bandwidth. This structure may need a high-pass filter with equalization and can potentially lead to the saturation of the amplifier. The high-impedance design may also suffer from an increased sensitivity to C_{D} (Park & Toumazou 1997). Correspondingly, the low-impedance approach has high bandwidth and high dynamic range at the price of lower sensitivity and higher noise (Kamrani et al., 2013).

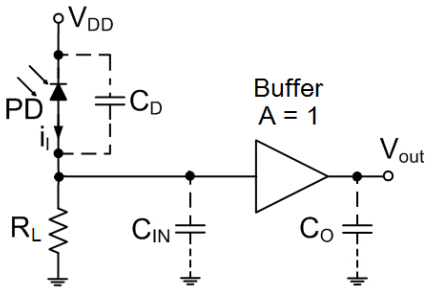

Fig. 1.2. Low impedance front-end TIA

In spite of their limitations, due to their simplicity, the approaches can be still useful in special applications where the technology constraints prevent more complex designs from being used. A simple calculation can demonstrate that under some circumstances a TIA with almost zero power consumption can be designed to directly convert the PD's current to logic levels. Unfortunately, for practical gain and bandwidth requirements, the input capacitance shall be unrealistically small and this limits the applicability of such designs.

B. Resistive Shunt Feedback TIA

As we have seen before, the simplest design results in a direct trade-off between the noise and the bandwidth, which is not easy to overcome. Clearly, a different and somehow more complex design may be necessary to mitigate some of the shortcomings of simple high- and low- impedance front-ends. Any discussion on CMOS TIAs shall, probably, start with a classical resistive SFB TIA shown in Fig. 1.3. The design results in low input impedance, as is beneficial for a current sensing block (Royo et al., 2016) and, at the same time, low output impedance as is important for voltage output amplifiers (Shahdoost et al., 2014). Note that input impedance has to be low in order to deal effectively with large external PD capacitance as is important for the envisioned OTDR instruments served with off-chip detectors. The architecture is rather commonly used because R_{F} does not carry a large bias current and therefore its value can be maximized (Razavi, 2000). Furthermore, the feedback topology can be utilized to help maximize feedback resistance without having constraints for voltage headroom as may be in the case for feed-forward amplifier configurations.

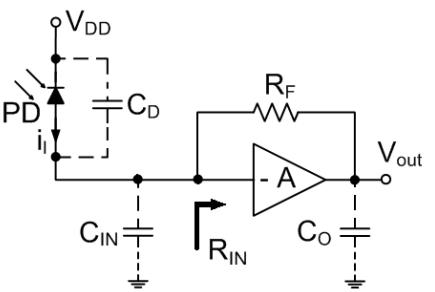

Fig. 1.3. Basic configuration of a resistive feedback TIA

In the basic version of this TIA topology, the frequency-dependent transimpedance becomes (Salhi et al., 2017):

$$Z_{\mathrm{T}}(s) = -\frac{A}{A+1}\frac{R_{\mathrm{F}}}{1+\frac{R_{\mathrm{F}}C_{\mathrm{T}}}{A+1}s}, \tag{1.8}$$

where the mid-band transimpedance gain R_{T} can be approximated as:

$$R_{\mathrm{T}} = -\frac{A}{A+1} R_{\mathrm{F}}. \tag{1.9}$$

For sufficiently large values of the open-loop gain $A \gg 1$, we get approximately $R_{\mathrm{T}} \approx -R_{\mathrm{F}}$ for low frequencies. The -3 dB bandwidth of the design becomes correspondingly:

$$BW_{-3\mathrm{dB}} = \frac{1}{2\pi R_{\mathrm{IN}} C_{\mathrm{T}}}, \tag{1.10}$$

where R_{IN} is the input resistance of the circuit and C_{T} is the total input capacitance. Here the PD is modeled as a current source in parallel with the capacitance C_{D}. For the general frequency-dependent transimpedance gain the dominant pole is defined by $R_{\mathrm{F}} C_{\mathrm{T}}$ and this limits the bandwidth of the system (Momeni et al., 2010). For high-frequency applications, while the dominant pole of the open-loop frequency response is located at the input node because of the total input capacitance C_{T}, the remaining poles of the amplifier must be located above the cut-off frequency as non-dominant poles to ensure good stability (Salhi et al., 2017). As the following holds:

$$R_{\mathrm{IN}} = \frac{R_{\mathrm{F}}}{A+1}, \tag{1.11}$$

and $C_{\mathrm{T}} = C_{\mathrm{D}} + C_{\mathrm{IN}}$, one easily obtains:

$$BW_{-3\mathrm{dB}} = \frac{A+1}{2\pi R_{\mathrm{F}} C_{\mathrm{T}}} = \frac{A+1}{2\pi R_{\mathrm{F}} \left(C_{\mathrm{D}} + C_{\mathrm{IN}}\right)}. \tag{1.12}$$

Here for the fixed PD capacitance, the value R_{F} is directly proportional to the gain and inversely proportional to the bandwidth. Clearly, the bandwidth can be improved by increasing the open-loop gain of the amplifier.

The low frequency input-referred noise current is given by:

$$\overline{i^2_{\mathrm{n,TIA}}} = \overline{i^2_{\mathrm{n,R_F}}} + \overline{i^2_{\mathrm{n,A}}} = \overline{i^2_{\mathrm{n,R_F}}} + \frac{\overline{v^2_{\mathrm{n,amp}}}}{R^2_{\mathrm{F}}} = \frac{4\mathrm{k_B}T}{R_{\mathrm{F}}} + \frac{4\mathrm{k_B}T\gamma}{g_{\mathrm{m}} R^2_{\mathrm{F}}}, \tag{1.13}$$

while the equivalent noise power at the input can be shown to be (Hammoudi & Mokhtar, 2010):

$$\overline{I^2_{\mathrm{n,TIA}}} = \frac{4\mathrm{k_B W}T}{R_{\mathrm{F}}} BW + 2qI_{\mathrm{G}} BW + 2qI_{\mathrm{dark}} BW + \frac{8\mathrm{k_B}T}{3g_{\mathrm{m}}} \left[\frac{BW}{R^2_{\mathrm{IN}}} + \left(2\pi C_{\mathrm{T}}\right)^2 BW^3\right], \tag{1.14}$$

where B is the useful bandwidth, I_{G} is the gate current, I_{dark} is the dark current of the PD and q is the electron charge.

Obviously, the input-referred amplifier noise is passed to the input by scaling it with R_{F}^2 and the overall input-referred noise current is roughly equal to the one of an impedance front-end TIA. From the design, it becomes clear that this TIA benefits from low noise of a large R_{F} without the drawback of slow response as it was for an impedance TIA. In other words, if one lets, for example, $R_{\mathrm{F}} = R_{\mathrm{L}}$, both the impedance TIA and SFB TIA would possess roughly equal transimpedance gain R_{T} and noise current $\overline{i_{\mathrm{n,TIA}}^2}$, but the latter configuration would also get a factor $A + 1$ larger bandwidth. Recall that even though one can try to reduce the input noise by increasing R_{F}, the implementation of large resistors not only consumes huge area, but may also introduce significant parasitic capacitances which may degrade the speed. Alternatively, one can use pseudo-resistors instead of large resistances in order to decrease both the area and parasitics, but those tend to be very non-linear and complex designs and the technological process change may be needed (Rajabzadeh et al., 2018).

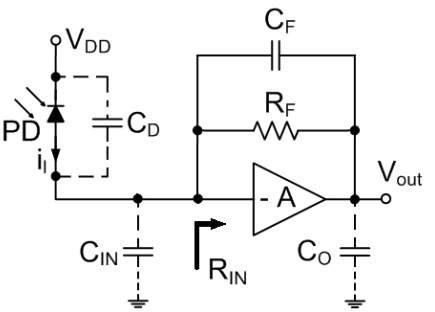

Fig. 1.4. Resistive feedback TIA with an additional feedback capacitor

For example, a classical SFB TIA as described above can also have stability issues when designed to work with large PDs of different capacitances and C_{D} can also significantly limit the bandwidth of the circuit as well as its noise performance (Park et al., 2007; Shahdoost et al., 2014). Furthermore, with typical speed, headroom and power constraints the input transistor may contribute as much input noise as R_{F} does (Razavi, 2000).

Often, a dedicated compensation C_{F} is added in parallel with the feedback resistor R_{F} to achieve the maximally flat response (see Fig. 1.4). Although this additional feedback capacitor can also reduce the amplifier's sensitivity to varying values of C_{D} (exactly this behavior was employed in (Yeom et al., 2019) while designing the OTDR ASIC.) and to improve the instability (Wilson & Chen, 2014), it also reduces the maximum achievable R_{T} and therefore may not always be the best option. In the case of the C_{F} it can be shown that the frequency-dependent

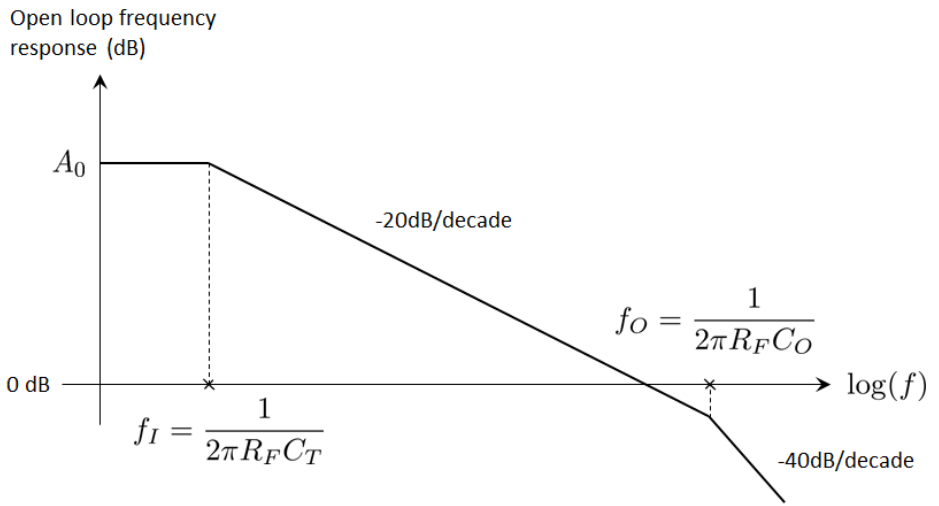

Fig. 1.5. Open loop frequency response for a second-order SFB TIA

transimpedance becomes (Yeom et al., 2019):

$$Z_{\mathrm{T}}(s) = -\frac{R_{\mathrm{F}} A\beta}{A\beta + 1}, \tag{1.15}$$

where

$$\beta = \frac{1 + R_{\mathrm{F}} C_{\mathrm{F}} s}{1 + R_{\mathrm{F}}(C_{\mathrm{T}} + C_{\mathrm{F}})\, s}. \tag{1.16}$$

Within the analysis as above, the amplifier pole was neglected assuming that it is much higher than the closed-loop input pole (i.e. infinite-bandwidth amplifier). However, for high-speed applications, where the speed of the TIA also goes quite high, this assumption may be violated and it is more realistic to assume a single-pole amplifier which is a good approximation of a simpler single-stage amplifier. In that case the amplifier pole can have an impact on the closed-loop behavior of the system and, eventually, can even limit the bandwidth of the circuit. Here we assume that the core voltage amplifier has a single pole at f_0 at the presence of the output capacitance C_{O}. If the input pole and the output poles are close enough, the system can have stability issues. The open-loop response for such a second-order system is shown in Fig. 1.5. In a second-order system like this one has to watch out for an undesired peaking in the closed-loop frequency response.

Then the closed-loop transimpedance becomes:

$$Z_{\mathrm{T}}(s) = \frac{-R_{\mathrm{T}}}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1} = -\frac{A}{A+1} \frac{R_{\mathrm{F}}}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1}. \tag{1.17}$$

In the expression above ω_0 is the angular frequency of the pole pair:

$$\omega_0 = \sqrt{\frac{A+1}{R_\mathrm{F} C_\mathrm{T} T_\mathrm{A}}}, \tag{1.18}$$

Q is the quality factor of the pole pair:

$$Q = \frac{\sqrt{(A+1)\, R_\mathrm{F} C_\mathrm{T} T_\mathrm{A}}}{R_\mathrm{F} C_\mathrm{T} + T_\mathrm{A}}, \tag{1.19}$$

and T_A is the time constant of the high frequency pole, where the quality factor Q is related to the damping factor ζ as:

$$Q = \frac{1}{2\zeta}. \tag{1.20}$$

When Q is equal to $1/\sqrt{3}$, one gets Bessel response, which gives maximally flat group-delay characteristics. When Q is $1/\sqrt{2}$, one gets Butterworth response with maximally flat frequency response and no peaking. Larger Q will give rise to peaking in frequency response. If the Butterworth response[3] is the design target, one obtains:

$$f_\mathrm{O} \approx \frac{A}{\pi R_\mathrm{F} C_\mathrm{T}}. \tag{1.21}$$

This time the bandwidth becomes:

$$BW_{-3\mathrm{dB}} = \frac{\sqrt{2A\,(A+1)}}{2\pi R_\mathrm{F} C_\mathrm{T}} \approx \frac{\sqrt{2}A}{2\pi R_\mathrm{F} C_\mathrm{T}}, \tag{1.22}$$

or when the feedback capacitor is included:

$$BW_{-3\mathrm{dB}} = \frac{\sqrt{2A\,(A+1)}}{2\pi R_\mathrm{F}\,(C_\mathrm{T} + C_\mathrm{F})} \approx \frac{\sqrt{2}A}{2\pi R_\mathrm{F}\,(C_\mathrm{T} + C_\mathrm{F})}. \tag{1.23}$$

Compared to the TIA with an infinite-bandwidth voltage amplifier, one can find out that the TIA bandwidth is increased by approximately factor of $\sqrt{2}$. Saying differently, if one starts with a very wideband voltage amplifier and then reduces its bandwidth (e.g. by loading it with a capacitor) to its optimum value, the TIA's bandwidth improves by about 40%. This can be qualitatively explained by the fact that the real poles become complex poles and Q goes higher. In other words, the pole introduced by the core amplifier creates an effective inductive behavior in the

[3]The broadband Butterworth characteristics (maximum flatness) is typically the most desirable one for TIA circuit design (Jia Xu & Zhenghao Lu, 2011).

input impedance of the TIA by partially cancelling the roll-off due to the input capacitance. Note, however, that further increasing T_{A} (decreasing f_{O}) will reduce this bandwidth boost effect quickly and will lead to the peaking in frequency response.

If one limits the analysis to the TIA designs which are free of amplitude peaking (e.g. Butterworth, Bessel and critically damped), one obtains the following inequality which is known as the transimpedance limit for the second-order system:

$$R_{\mathrm{T}} \leq \frac{Af_{\mathrm{O}}}{2\pi C_{\mathrm{T}} BW_{-3\mathrm{dB}}^2}, \tag{1.24}$$

where Af_{O} represents the gain-bandwidth product of the single-pole voltage amplifier and which is roughly constant for the given technology. The transimpedance limit predicts a rapid noise growth for wider bandwidth making the SFB TIA less attractive for high-speed applications. Furthermore, in advanced CMOS technology, the lower V_{DD} further limits the attainable A with one stage voltage amplifier. Of course, cascading more gain stages can boost amplifier gain, but it will also make it difficult to ensure sufficient phase margin and, therefore, often a single-stage core amplifier is employed in these designs.

Another interesting option was suggested in (Woo et al., 2017), where a variable T-network was implemented in place of the feedback resistor using variable floating resistor with 10-bit current steering DAC. The floating resistor allows the amplifier to obtain both excellent output linearity and wide dynamic range, where an integrated digital controller of the current generator lowered the TIA noise by reducing the amount of fluctuation in the floating resistor (Woo et al., 2017).

Another typical design is to use the SFB TIA with the feedback from the source follower as elaborated in (Keshri, 2010). Both designs result in the same transimpedance gain, while the version with feedback from the source follower has smaller input resistance and hence, higher bandwidth. On the other hand, the input-referred noise contribution is smaller in the version without the source-follower.

C. Inverter-Based Feedback TIA

In general, there is a certain flexibility in the design of the voltage amplifier. Usually, challenged by the requirements of the noise performance, a simpler voltage amplifier with less active components is opted (Shahdoost et al., 2014) leading to a smaller input current noise. A basic TIA design can use a single-stage voltage amplifier if sufficient gain can be realized (Shahdoost et al., 2016). The choice of the topology for the input voltage amplifier is mainly dictated by the noise requirements as well as those of bandwidth.

The push-pull inverter-based approach (see Fig. 1.6 (a)) can be considered as a special case of the SFB TIA where the push-pull inverter is used to maximize the

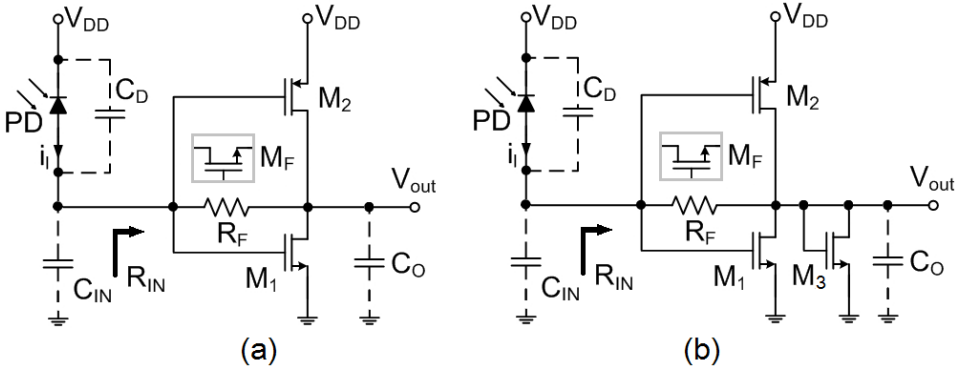

Fig. 1.6. Push-pull inverter based TIA: (a) design with resistive feedback; (b) modification with an active load

amplifier transconductance (Hammoudi & Mokhtar, 2010). Although the inverter configuration of the TIA was among the earliest employed, due to its simplicity it is still often used with numerous modifications reported. One of the main advantages of the inverter-based design is that both NMOS and PMOS transistors reuse the same drain current which results in lower power dissipation (Dash et al., 2013). Although it is configured as a digital inverter, the operating point is selected so that both transistors are in saturation mode resulting the inverter to be in its high gain region. The open-loop gain of such push-pull inverter can be shown to be (Escid et al., 2013; Salhi et al., 2017):

$$A = -\frac{g_{\mathrm{m},1} + g_{\mathrm{m},2}}{g_{\mathrm{ds},1} + g_{\mathrm{ds},2}} = -\frac{g_{\mathrm{m}}}{g_{\mathrm{ds}}}, \tag{1.25}$$

where $g_{\mathrm{m}} = g_{\mathrm{m},1} + g_{\mathrm{m},2}$ and $g_{\mathrm{ds}} = g_{\mathrm{ds},1} + g_{\mathrm{ds},2}$ correspond to the total transconductance and conductance of the push-pull inverter. The low-frequency transimpedance gain becomes (Zohoori & Dolatshahi, 2018):

$$R_{\mathrm{T}} = R_{\mathrm{F}} \frac{g_{\mathrm{m},1} + g_{\mathrm{m},2}}{g_{\mathrm{ds},1} + g_{\mathrm{ds},2}} = R_{\mathrm{F}} \frac{g_{\mathrm{m}}}{g_{\mathrm{ds}}}. \tag{1.26}$$

This topology exhibits a lower input-referred noise current when compared to resistive shunt-feedback approach at the price of higher input capacitance (Razavi, 2019). In order to optimize the noise one may be willing to replace the R_{F} with the MOSFET device in the triode region, where the effective resistance can be adjusted via the gate-to-source bias voltage V_{gs}:

$$R_{\mathrm{F}} = \frac{1}{\frac{W}{L}\mu C_{\mathrm{ox}} \left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)}, \tag{1.27}$$

where W is the gate width, L is the gate length, C_{ox} is the gate oxide capacitance per unit area, μ is the charge-carrier effective mobility, V_{th} is the threshold voltage of the device and V_{gs} is the gate-source voltage.

Although usage of the MOSFET looks attractive from a first glance, it may also have some disadvantages. For example, in the design of a variable-gain TIA reported in (Dash et al., 2013), the authors claimed that the MOSFET operating in the triode region may suffer from severe global process variations when the overdrive voltage becomes too low (i.e. when R_{F} is increased). The architecture with a push-pull inverter may serve as a good basis for an extremely low-power amplifier. The work (Dash et al., 2013) reported 0.32 mW for a version with 0.85 GHz bandwidth. Compared to classical CS-based resistive feedback TIA, the inverter configuration also possesses a superior capability to accommodate larger input currents.

At the same time, usage of an inverter-based amplifier may become problematic for applications above several GHz as reported in (Wu et al., 2005) due to low-speed properties of the inverter-configuration TIA. Numerous modifications of this simple topology have been demonstrated in order to address bandwidth limitations. For example, the authors in (Hammoudi & Mokhtar, 2010; Liu et al., 2015; Singh et al., 2012) and (Escid et al., 2013) replaced a single push-pull inverter with multiple cascaded stages (correspondingly three or five) to achieve higher gain, while the authors in (Aziz et al., 2018; Hammoudi & Mokhtar, 2010; Liu et al., 2015; Singh et al., 2012) also employed an active load M_3 in every stage to increase the bandwidth and to minimize the Miller effect (see Fig. 1.6 (b)). In this case, the amplifier transistors can be also made larger to avoid overshoot (Liu et al., 2015). Some modifications with single or multiple inductive-series peaking were also reported (Liu et al., 2015; Wu et al., 2005). Clearly, combinations of inverter and CS-based stages are also possible. For example, some authors reported on a high dynamic range three-stage TIA cascode inverter as input stage and two CS stages with the feedback resistor spanning all three stages (Hassan & Zimmermann, 2011).

Interesting modifications of the classical push-pull inverter-based TIA were proposed in (Zohoori & Dolatshahi, 2018; Zohoori et al., 2019a). For example, in (Zohoori et al., 2019a) diode-connected transistors M_{11} and M_{12} are added to the input node to decrease the input resistance (see Fig. 1.7). According to the authors, this results in moving the dominant pole to the higher frequencies and sets the required DC voltage bias at the input node, thus considerably extending the bandwidth of the amplifier. Alternatively, cascode transistors can be also added to transistors M_1 and M_2. In this way, not only the Miller capacitance is eliminated, but also the output resistance is increased which also leads to the increase of the gain and decrease in power consumption as reduced DC current passes through the circuit.

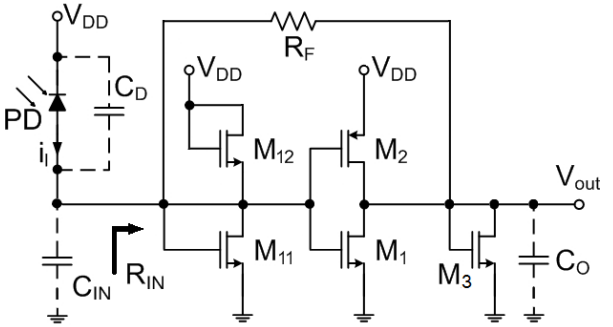

Fig. 1.7. Push-pull inverter-based TIA with resistive feedback and reduced input resistance according to (Zohoori et al., 2019a)

D. Common-Gate TIA

Unfortunately, not all inherent limitations of the classical resistive SFB TIA can be addressed with simple modifications of the reference architecture and adjustments on core voltage amplifier. For example, even if the feedback capacitor C_{F} can reduce the TIAs sensitivity to varying values of C_{D}, it also reduces the maximal achievable transimpedance Z_{T} and therefore is not always the best option.

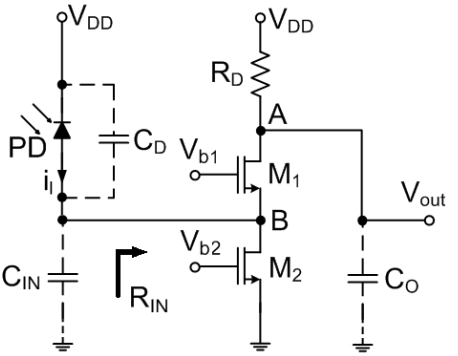

Fig. 1.8. Basic configuration of a common-gate TIA

The sensitivity to large input capacitance can be addressed by a so-called *feed-forward* CG TIA as shown in Fig. 1.8. The design allows isolating the PD's capacitance from the bandwidth determination by reducing the input impedance of the amplifier. The CG input stage presents a small input resistance:

$$R_{\mathrm{IN}} \approx \frac{1}{g_{\mathrm{m},1}}, \tag{1.28}$$

which moves the input pole to larger frequencies if the channel width of M_1 is

judiciously chosen. In some sense, this decoupling also eliminates the inherent trade-offs of the resistive feedback design as the parameters of the TIA can be determined independently from the input capacitance (Booyoung Choi et al., 2008; Kossel et al., 2003). If the output pole does not limit the bandwidth, one gets:

$$BW_{-3\mathrm{dB}} \approx \frac{1}{2\pi R_{\mathrm{IN}} C_{\mathrm{T}}} = \frac{g_{\mathrm{m},1}}{2\pi C_{\mathrm{T}}}. \tag{1.29}$$

Since all the signal current flows into the load resistor R_{D}, the mid-frequency transimpedance becomes trivially $R_{\mathrm{T}} = R_{\mathrm{D}}$. The thermal noise current from bias M_2 and the load resistor R_D are directly referred to the input resulting in:

$$\overline{i^2_{\mathrm{n,TIA}}} = \overline{i^2_{\mathrm{n,R_D}}} + \overline{i^2_{\mathrm{n,M_2}}} = \frac{4\mathrm{k_B}T}{R_{\mathrm{D}}} + 4\mathrm{k_B}T\gamma g_{\mathrm{m},2}. \tag{1.30}$$

The above expression does not include the noise contribution from M_1, since channel length modulation was not taken into account for simplicity. However, with the latter taken into account, it may lead to a noise current contribution term from M_1 as well (Keshri, 2010).

The architecture became relatively popular due to its inherent advantages for high-speed applications. The architecture helped to solve some of the problems typical for classical resistive feedback as it offers a reduction of power consumption and diminishes stability issues due to large input capacitance (Shahdoost et al., 2014). On the other hand, it also introduced drawbacks on its own such as an increase in noise levels.

The expressions for the mid-frequency transimpedance and noises clearly indicate that in order to achieve a higher gain and low noise, R_D shall be maximized. However, the maximum value of R_D is limited by the voltage headroom available and, as a result, for smaller technology nodes the topology may become limited by the gain. Additionally, increasing the value of R_D results in introducing pole with the load capacitance C_O which may result in lowering down the bandwidth (Keshri, 2010). As a consequence, the allowable headroom for M_2 is limited resulting in significant noise contribution. Here, too, for large transistors and/or large C_{D}, the noise contributed by M_1 may rise for high frequencies (Razavi, 2000). In the end, the noise of this topology is higher when compared to previously described CS-based SFB TIA as high thermal noise is also present in practical circuit realization. Additionally, the design offers fewer degrees of freedom for noise optimization when compared to classical SFB TIA and with the same technology and bandwidth, feed-forward TIA will always have lower transimpedance when compared to the feedback approach (41% less transimpedance gain at its best condition when compared to the SFB TIA (Hosseinisharif et al., 2020)). The expression for input-referred noise current becomes even worse when all parasitic capacitances

are taken into account at high frequencies (Keshri, 2010).

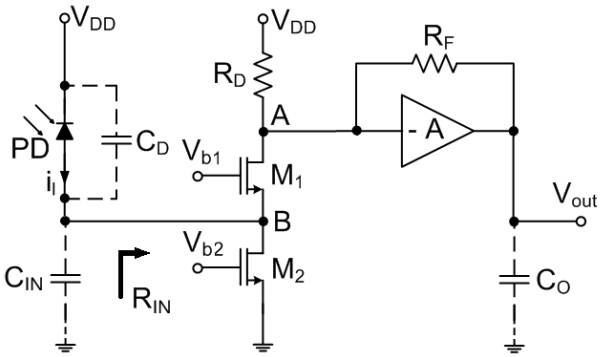

Fig. 1.9. TIA with CG as an input stage

Nevertheless, combinations of feed-forward and feedback approaches are possible and even strongly suggested by some authors. Here the transimpedance limit can be circumvented by decoupling the PD with the CG input stage similarly to the one shown in Fig. 1.9 (Booyoung Choi et al., 2008; Park et al., 2007). The CG input stage acts as a current buffer and ensures a small input resistance. The input pole can be moved to a higher frequency and thus the dominant pole of the circuit is now located at node A (Park et al., 2007). The TIA itself can be modified (e.g. using shunt-peaking or other techniques) to obtain an improved performance with the overall transimpedance gain being roughly equal to R_{F} if R_D is much larger than $R_{\mathrm{F}}/\left(A+1\right)$. Now the sensitive feedback node of the transimpedance stage is more robust compared to a classical design as its poles are not determined by any off-chip components. Furthermore, the CG stage permits the transistors of the following transimpedance stage to be sized smaller making higher transimpedance values possible. Although such a combined architecture allows effective C_{D} isolation, it may result in a significant increase of the power consumption compared to a feed-forward-only approach. Thus, it is believed to be better suited for bipolar rather than CMOS-based designs, since the superior g_{m} of the bipolar front-end leads to overall better performance (Park & Toumazou 1997). In terms of noise such a combined approach will not perform better than a pure CG front-end.

E. Regulated Cascode TIA

The RGC TIA is yet another concept that is famous for its extremely low input impedance and wide output voltage range (Han et al., 2010; Liu et al., 2012) with the structure shown in Fig. 1.10 (a). The RGC TIA is essentially a CG amplifier with local active feedback (Rani & Dhaka, 2014) and was sometimes referred under this name (Aflatouni & Hashemi, 2009). Here the common-gate stage, the transis-

tor M_1 together with the resistors R_D and R_S provide low input impedance, high bandwidth and moderate noise. The bias voltage of M_1 is provided by a voltage booster amplifier, implemented as, for example, a dedicated CS stage. Here, by exploring shunt-series feedback with booster amplifier, one is able to get even better C_{D} isolation when compared to the previously-discussed simpler CG approach.

The DC input impedance for the shown CS-based implementation becomes (Bashiri et al., 2010; Han et al., 2010):

$$R_{\mathrm{IN}} = \frac{1}{g_{\mathrm{m},1}\,(1+A)} = \frac{1}{g_{\mathrm{m},1}\,(1+g_{\mathrm{m},2}R_2)}, \tag{1.31}$$

where $A = g_{\mathrm{m},2}R_2$ is the gain of the CS stage for the demonstrated approach in Fig. 1.10 (b). In order to maintain the low input impedance, $g_{\mathrm{m},1}$ has to be maximized either by increasing the bias current or by increasing the width of M_1 (Bashiri et al., 2010). However, increasing the current also creates a voltage headroom problem and increases the input-referred noise. On the other hand, increasing the width of M_1 increases both its input and output capacitance. Clearly, another way to keep the input resistance small is to increase the product of $g_{\mathrm{m},2}R_2$. Unfortunately, both M_1 and M_2 are biased through R_2, so a special care may be needed if one decides to increase R_2 (Bashiri et al., 2010).

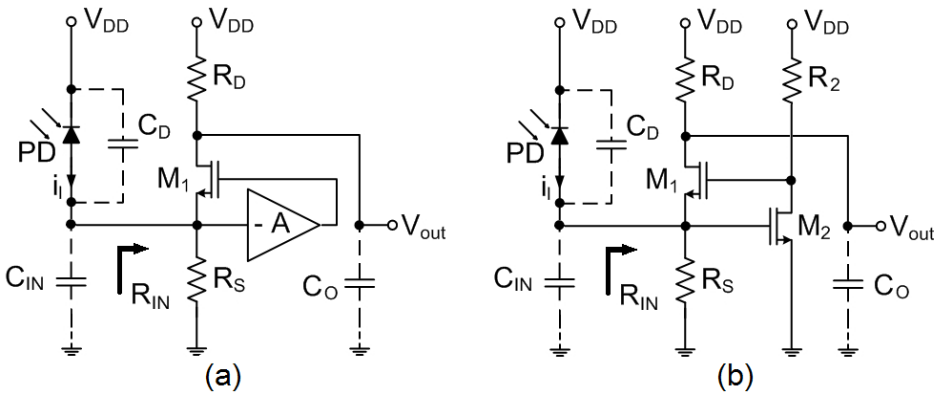

Fig. 1.10. Regulated cascode TIA: (a) general concept; (b) the simplest implementation with voltage amplifier as a CS stage

Due to the booster amplifier, the input resistance of this design is a factor $(1 + A)$ smaller compared to CG TIA, which allows the designs with smaller transistors and reduced power consumption. Similarly to CG configuration, the mid-frequency transimpedance gain is also $R_{\mathrm{T}} = R_D$. As we have seen above, in its simplest case, the bias stage of RGC can be implemented as a single stage CS voltage amplifier, although more advanced configurations are possible. For example,

the authors in (Soltanisarvestani et al., 2020) suggested improving the gain of the booster amplifier by adding a cascode transistor on the top of M_2, while (Atef & Zimmermann, 2012) suggested using a push-pull inverter in place of the reference CS-based solution.

Note that for circuits designed to operate from the low supply voltage (such as 1.0 V in (Szilagyi et al., 2014)) even a classical single-transistor CS-based approach may not work or will produce insufficient gain and alternative solutions shall be found (Hosseinisharif et al., 2020). Furthermore, RGC TIA is often behaving as a current buffer designed for smaller gain and a dedicated voltage gain stage is added (Mekky et al., (2013); Soltanisarvestani et al., (2020)). The provision of the extra gain can be implemented similarly to the approach shown in Fig. 1.9 for CG input stage (Ngo et al., 2010), where for bandwidth enhancement, a shunt-shunt feedback resistor R_{F} is applied to move the dominant pole of the amplifier to a higher frequency. Here a large pole spacing and higher Z_{T} may be achieved at the expense of increased power dissipation.

It had been also shown that RGC configuration results in smaller noise when compared to CG approach (Han et al., 2010). An interesting comparison of current-mode TIA was demonstrated in (Booyoung Choi et al., 2008), where CG and RGC were designed for similar target specifications and their performance was compared. The authors demonstrated that RGC design resulted in a larger gain, larger bandwidth than the CG-based design while, at the same time, operating with three times larger input capacitance (e.g. 2 pF vs. 6 pF). This clearly demonstrated the superiority of the RGC-based approach over an equivalent CG-based with only a marginal increase in the current consumption. One interesting application area of these high-speed feed-forward topologies are those where one has to sustain the oscillation condition in the loop. This requires a zero phase shift at the desired resonance frequency over the loop which also imposes a stringent bandwidth specification, especially for higher frequencies (Mekky et al., 2013). To guarantee zero phase shift over the loop, the bandwidth is set to be at least ten times the expected resonance frequency with an interesting application for MEMS capacitive resonators shown by the authors. Although both CG and RGC topologies may look like good candidates for relaxing the effect of the input capacitance, their high current noise contribution of the load and input transistors significantly degrade the noise performance. Therefore, these architectures can be hardly considered as suitable candidates for envisioned low-noise applications (Shahdoost et al., 2014).

F. Flipped Voltage Follower TIA

The FVF topology is shown in Fig 1.11 and can serve as a basis for very compact designs as it uses only three active devices (Monsurro et al., 2010). The circuit has only one current branch and exploits feedback to reduce both its input and output impedances. Here the transistor M_1 is biased in the triode region, whereas

both M_2 and M_3 are biased in saturation. The bias voltage of M_2 controls the transimpedance gain, while the bias voltage for M_3 determines the bias current itself (Monsurro et al., 2010). Under some rather mild assumptions, it can be shown that the low-frequency transimpedance is equal to the inverse transconductance of M_1:

$$R_{\mathrm{T}} \approx \frac{1}{g_{\mathrm{m},1}}. \tag{1.32}$$

The results in (Monsurro et al., 2010) show that FVF has similar input impedance, noise and bandwidth to that of RGC when both designed for the same gain and power consumption. The topology is well-suited for low-power and high-density applications. Unfortunately, its noise performance is similar to the one of the previously discussed RGC design.

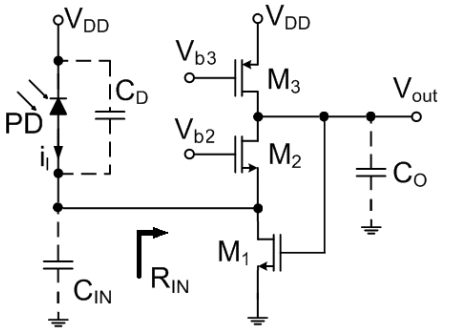

Fig. 1.11. General concept of flipped voltage follower TIA

G. Inductive Enhancement

Even though the inductors have been historically associated with narrow-band circuits, they appeared to be useful in broad-circuits as well (Mohan et al., 2000). Monolithic inductors have opened up new possibilities for wide-band circuit design and had been intensively employed in developing modern circuits where the inductor is used to tune out the capacitance in order to boost both the transimpedance and the bandwidth of the TIA circuit.

As we have seen above, even though CG and RGC schemes can effectively isolate large input capacitance effect in order to increase the bandwidth, their noise performance is often insufficient (Atef & Abd-elrahman, 2014). Here an inductive peaking is another approach to increase the bandwidth which has been widely adopted for low-voltage low-power broadband amplifiers. The general idea of the method is to allow the bandwidth limiting capacitance to resonate with the inductor, thus increasing the overall speed of the circuit (Han et al., 2010). The TIAs with inductor peaking mainly differ in the way the inductors are mounted

to expand the bandwidth of the circuit. Several approaches are known such as feedback peaking inductor (Salhi et al., 2017), shunt peaking (Mohan et al., 2000; Yong-Hun Oh & Sang-Gug Lee, 2004), single or multiple inductive series peaking (Escid et al., 2013; Wu et al., 2005), π-type inductor peaking (PIP) (Jin & Hsu, 2006, 2008a,b) or different combinations of them (Aflatouni & Hashemi, 2009; Chao-Yung Wang et al., 2007). For example, by using an inductive shunt peaking at the output of TIA one is able to improve the bandwidth by adding a zero to the transfer function. Similarly, an addition of the inductor to the gate of the output transistor in RGC configuration implements inductive peaking by adding a pair of complex conjugate poles (Aflatouni & Hashemi, 2009). Depending on the type of inductive peaking, one may theoretically achieve a bandwidth enhancement as high as factor 3.46, although the discrepancies in the real circuit and the assumptions on the parasitic capacitances may degrade the expected gain in bandwidth. A clear advantage of the inductor peaking TIA is that the bandwidth increase often comes with no additional power dissipation (Mohan et al., 2000; Yong-Hun Oh & Sang-Gug Lee, 2004), while the flatness of the frequency response is typically (but not necessarily) sacrificed.

On-chip inductors are typically realized either by using the bond wires or on-chip spirals. Because the bond-wires may exhibit much higher quality factors when compared to the spiral inductors, their usage may be constrained by the limited range of the realized inductances and large production fluctuations (Mohan et al., 2000). Furthermore, the bond-pad capacitance may also degrade the performance of such an inductor. According to (Mohan et al., 2000), differential implementation of such amplifiers may lead to a degradation in power supply rejection ratio due to a possible mismatch between the two bond-wires. The spiral on-chip inductors usually exhibit good matching and could have been more suitable for envisioned differential architecture of the OTDR TIA. Although these inductances also allow a larger range of values to be realized, they may possess smaller quality factors and have been historically harder to model as was elaborated in the seminal work of Mohan. In practice, the inductor design problem often boils down to choosing the geometrical parameters of the spiral such as the desired inductance is obtained while the parasitic capacitance is minimized.

Modern CMOS processes often provide up to eight metal layers which can be used to form a number of useful structures including inductors (Razavi, 2002). Furthermore, multiple available metal layers ensure flexibility in stacked inductor design and can result in significant area savings when the vertical spacing between spirals is used. Thanks to the extensive work on monolithic inductors in RF design, the inductive peaking can be now realized with an accurate prediction of the inductor's performance even for optical communication circuits. The inductors with quality factors Q as low as 3-4 with simple compact spiral structures have proved to be adequate for increasing the bandwidth (Razavi, 2002).

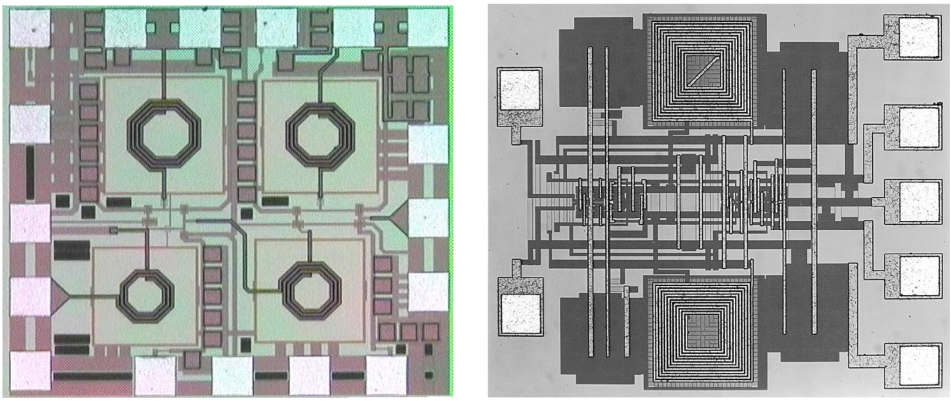

Fig. 1.12. Chip photographs with examples of on-chip inductors: (a) two-stage TIA with combined series- and shunt-peaking reported in (Chao-Yung Wang et al., 2007); (b) TIA with highly optimized planar spiral inductors from (Mohan et al., 2000)

However, the use of inductors to increase the bandwidth of an amplifier has a number of significant disadvantages. First of all, the usage of inductors with a standard CMOS dramatically increases the chip size and therefore makes associated hardware costs very high especially when one addresses cheap devices (Atef & Abd-elrahman, 2014) (see Fig. 1.12 for examples of chip die photos and relative area of the TIA chips occupied by passive inductors). This argument, however, may no longer be so critical, since the optimized shunt peaking on-chip inductors may consume only a fraction (e.g. 15%) of the total chip area (Mohan et al., 2000). On the other hand, a large inductor not only occupies the large area but it may be also difficult to maintain its inductive characteristic within the whole bandwidth of interest. Furthermore, the substrate coupling typically increases through the inductors resulting in higher cross-talks when compared to inductor-less designs[4] (Atef & Abd-elrahman, 2014; Atef & Zimmermann, 2012). Finally, large group delay fluctuations can become also problematic (Atef & Zimmermann, 2013) and the performance of TIA with inductor peaking may also degrade in digital processes with thin metals and lossy passive components (Momeni et al., 2010).

For a classical TIA configuration with the inductance L placed before the input stage of the core amplifier with the gain A, the feedback resistor R_{F}, input

[4]Low substrate coupling is extremely important in multi-channel solutions where cross-talk between several parallel channels has to be minimized.

capacitance C_{IN} and PD capacitance C_{D} the bandwidth becomes (Liu et al., 2015):

$$BW_{-3\mathrm{dB}} = \frac{A+1}{2\pi R_{\mathrm{F}}\left(\frac{C_{\mathrm{D}}}{\alpha} + C_{\mathrm{IN}}\right)}, \tag{1.33}$$

where the coefficient α with $s = \mathrm{j}\omega$ is:

$$\alpha = 1 + s^2 C_{\mathrm{D}} L. \tag{1.34}$$

This simple example demonstrates how single series inductance reduces the effect of C_{D} on the dominant pole while increasing the bandwidth of the amplifier.

In a series of works (Jin & Hsu, 2006, 2008a,b) a multistage TIA design with six CS cascades and PIP bandwidth enhancement was proposed, where the bandwidth limitation is broken by three inductances composing a stage resonating with the intrinsic capacitances (see Fig. 1.13). The combination of three PIP inductors can create two zeros and two pairs of complex conjugate poles in the transfer function resulting in significantly enhanced bandwidth. In Fig. 1.13 also a difference between the drain resistors R_D and matching resistors R_M at the input and output stages of the TIA is shown. According to the authors, the design does not disturb the low-frequency gain of the circuit and only affects the response within the higher frequency range, while the DC power consumption remains unchanged compared to the baseline CS amplifier without the PIP inductors. There may be also an optimal number of stages that maximizes the gain-bandwidth product to the total power consumption (Jin & Hsu, 2008b). According to the authors, the design also possesses an advantage as the capacitive loading from PD, which often limits the bandwidth of the amplifier, can be made by the proposed configuration to resonate resulting in a wider bandwidth of the circuit.

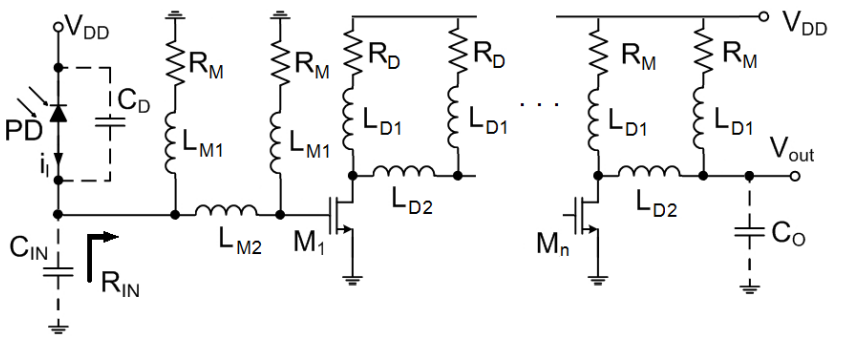

Fig. 1.13. A concept of multiple CS cascades with PIP bandwidth enhancement

An example of a simple bandwidth enhancement technique for push-pull inverter-based TIA is shown in Fig. 1.14 (a), where inductance is placed in the feedback path (Salhi et al., 2017). In (Escid et al., 2013) the authors offered a different concept, where a five-stage cascaded push-pull inverter was suggested with the inductance placed not in the feedback, but in series only before the last fifth stage. According to the authors, in this configuration, the inductance plays the role of a low-pass filter and absorbs parasitic capacitances. A similar approach was suggested in (Wu et al., 2005), where multiple inductive-series peaking was also used in multi-stage inverter-configuration TIA. According to the authors, the proposed series-peaking TIA manifests larger bandwidth and is less sensitive to the on-chip inductor quality factor. This is different to the inductive shunt-peaking technique which is very sensitive to stray capacitance induced by spiral inductance. The concept of series inductive peaking in combination with push-pull inverter for a single stage is shown in Fig. 1.14 (b). Clearly, combinations of different approaches are also feasible. For example, Kossel et al., (2003) employed a combination of the shunt and series inductive peaking for bandwidth enhancement. Alternatively one can also try the so-called capacitive peaking. The peaking introduces an additional pole into the original amplifier design and can be used for adjusting the amplifier bandwidth without sacrificing the low-frequency transimpedance gain. Unfortunately, the technique did not get a wide adoption when compared to far more popular inductive peaking.

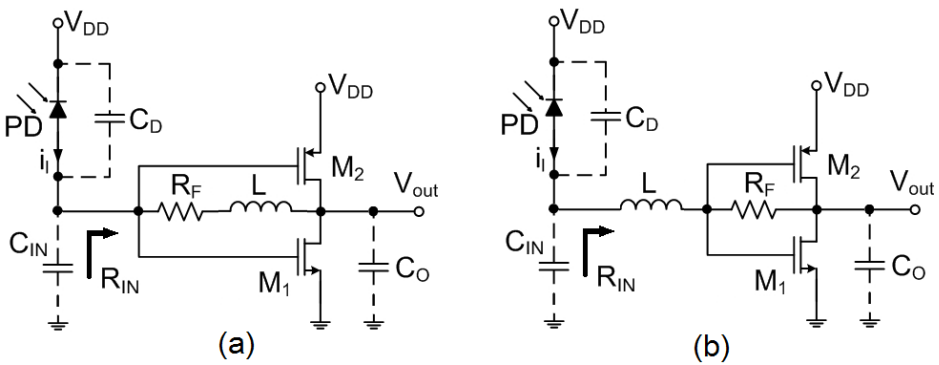

Fig. 1.14. Push-pull inverter-based TIA: (a) with feedback inductance; (b) with series peaking inductance

As a part of inductive enhancement, one can consider so-called input matching networks where a passive network is inserted between the PD and the TIA's input stage (Beaudoin & El-Gamal, 2002; Ngo et al., 2010). A somewhat disadvantage of this strategy is that the original TIA shall be first designed so that after the introduction of the matching network, the key requirements of the original specification

would be still satisfied. On the other hand, the method benefits from the fact that there is no need to change the structure of the TIA and only a passive network should be designed in addition to the main TIA part. Unfortunately, this network is able to deliver a perfect match only for a couple of discrete frequencies and the broadband noise matching can be hard to achieve while leading to response peaking and unwanted ripple. Still, some clever configurations are possible such as one reported in (Beaudoin & El-Gamal, 2002; Ngo et al., 2010), where the known bonding wire inductance was exploited as an element of the matching network to form a constant-k filter.

H. Active Inductor TIA

Even though a number of area-efficient designs for TIA with passive inductors have been reported, it is still difficult to integrate spiral inductors used in conventional circuits into CMOS technology. Moreover, the large parasitic capacitance of the spiral inductors may even reduce the bandwidth (Han et al., 2010). Note also that the conventional inductive shunt peaking technique is not very efficient under high-value load resistance of low-frequency applications (1-2 GHz range), since the amount of the required inductance is unrealistically high and is impractical for on-chip implementation (Yong-Hun Oh & Sang-Gug Lee, 2004). Active inductor TIA is yet another approach to increase the bandwidth and improve the sensitivity of the amplifier while avoiding the limitations of the passive inductors (Atef & Abd-elrahman, 2014). A concept of the active inductive load as a replacement of the resistive load is shown in Fig. 1.15. The active inductor consists of an NMOS transistor M, resistance R and capacitance C with the total impedance of the circuit (Atef & Abd-elrahman, 2014):

$$Z_{\mathrm{AI}}(s) = \frac{1 + sCR}{g_{\mathrm{m}}\left(1 + sC/g_{\mathrm{m}}\right)}. \tag{1.35}$$

The active inductor impedance for low-frequency is $1/g_{\mathrm{m}}$ and correspondingly R for high frequency. The inductive peaking occurs when $R \gg 1/g_{\mathrm{m}}$. According to (Atef & Abd-elrahman, 2014), the load acts as an inductor between the frequencies $\omega_1 = 1/CR$ and $\omega_2 = g_{\mathrm{m}}/C$ which are correspondingly zero and pole introduced by the active inductor. In the case of the CS-based SFB TIA, the transimpedance gain becomes approximately (Atef & Abd-elrahman, 2014):

$$Z_{\mathrm{T}}(s) \approx \frac{R_{\mathrm{F}}}{1 + \frac{sC_{\mathrm{T}}(Z_{\mathrm{AI}}(s)+R_{\mathrm{F}})}{g_{\mathrm{m},1}Z_{AI}(s)}}, \tag{1.36}$$

where $g_{\mathrm{m},1}$ is the transconductance of the transistor in the input CS stage.

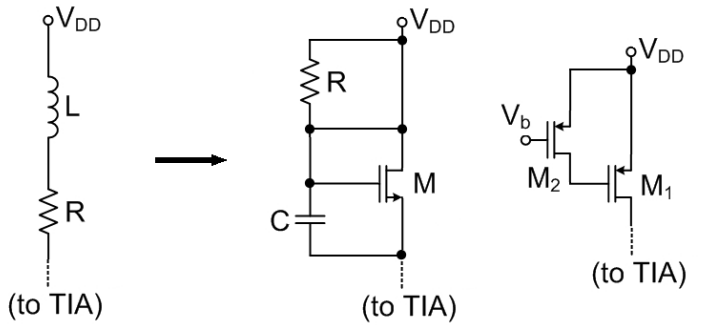

Fig. 1.15. A concept of the active inductor and alternative implementation using just two transistors

Similarly to a classical passive inductance, the technique reduces the effect of the input pole resulting in larger transimpedance gain and lower input noise current density when compared to a resistive load. Nevertheless, some works still prefer to employ classical inductances. For example, the authors in (Liu et al., 2015) have chosen an off-chip spiral inductor for their three-stage cascade push-pull inverter. The design provides higher inductance values for low-voltage high-speed circuits when compared to an equivalent active inductor circuit. Yet another issue with an active inductor is that it usually requires larger voltage headroom which may require itself either higher supply voltage or a dedicated voltage boosting technique (Abd-elrahman et al., 2016).

I. Capacitive Feedback TIA

As we have seen above, one of the main drawbacks of TIA architectures presented above is a poor noise performance. For example, in the most popular resistive feedback architecture current noise of the resistor is directly added to the input-referred current noise of the TIA which dramatically degrades the overall noise performance. Hence, one of the solutions to reduce the noise of the circuit is to replace the noisy feedback resistor with a noise-free circuit such as a capacitor. Such a circuit would eliminate the disadvantages of typical resistive feedback while maintaining the advantages due to the circuit's feedback structure.

An attempt to address the typical problems of previously discussed designs by using a so-called capacitive feedback TIA had been first reported in the seminal work of Razavi (Razavi, 2000) and elaborated in the series of works (Shahdoost et al., 2014; Shahdoost et al., 2014, 2011, 2016). The general circuit topology of such TIA is shown in Fig. 1.16.

In this topology, the amplifier maintains a virtual ground at the input node and hence the signal current flows through C_2. The capacitor C_2 senses the voltage across the first feedback capacitor C_1 and the current proportional to the sensed

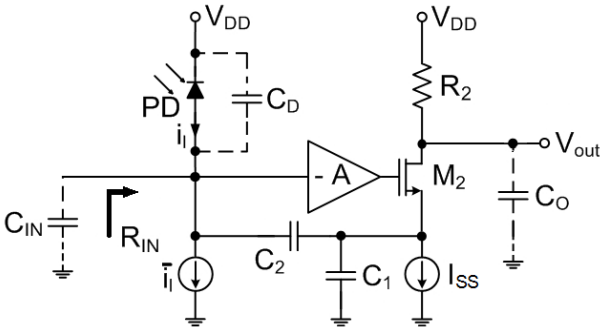

Fig. 1.16. Basic configuration of capacitive feedback TIA

voltage is returned to the input of the amplifier. Under the assumption of the high gain of the operational amplifier $A \gg 1$, the resultant current gain can be approximated as:

$$\frac{I_{\text{out}}}{I_{\text{in}}} \approx 1 + \frac{C_1}{C_2}. \tag{1.37}$$

This forms a current amplifier and, with the resistor R_2 connected to the drain of the output transistor M_2, the transimpedance gain for low frequencies becomes:

$$R_{\text{T}} = \left(1 + \frac{C_1}{C_2}\right) R_2 \approx \frac{C_1}{C_2} R_2, \tag{1.38}$$

for large ratio C_1/C_2. Here the capacitive term augments the gain of the resistor and allows for a larger combined on-chip gain. Important is that the capacitive gain does not contribute noise, while the noise current of the R_2 is divided by the current gain factor as we will see later. More detailed analysis also implies that, at least in general, the bandwidth can be increased via the increase of the gain of the core voltage amplifier without reducing R_2 and, therefore, without a negative impact on the transimpedance gain (Hu et al., 2010b).

The topology is believed to possess three major advantages over classical TIA designs. First of all, the gain definition network consisting of capacitances C_1 and C_2 contributes no noise. Furthermore, the capacitance as seen at the input node to ground lowers the DC loop gain rather than degrades the stability. Finally, the total noise current contributed by the first stage is significantly lower than the one in classical resistive-feedback TIA for the frequencies of interest and given bandwidth. Besides, the authors claim the system's gain is due to the ratio of two main capacitors which makes the overall design less vulnerable to the process variations when compared to the case when the absolute value of the resistance is used. Still, several significant circuit-level adjustments may be needed to produce a functioning design. Furthermore, the simplistic expressions above and the corresponding

arguments are only valid under conditions such as $C_{\mathrm{T}} \gg C_2$, perfect biasing and current sources and these assumptions may be easily violated when the circuit has to be implemented under realistic technological constraints.

J. Dynamic Range Enhancement, Programmable/Variable-Gain TIA

In optical sensing applications, a high dynamic range is often an essential requirement. The dynamic range is defined by the ratio of the maximum and minimum detectable current, where the upper limit is set by the maximum detectable current, whereas the minimum current is equivalent to the input-referred noise current (Hassan & Zimmermann, 2011). Besides low-noise and broadband applications, in short-haul optical systems where expensive EDFA is not present or in systems with the burst-mode operation, TIAs are also required to work under input overload conditions (Jia Xu & Zhenghao Lu, 2011). To meet these requirements, amplifiers with a built-in AGC circuit to adjust the conversion gain need to be employed reducing both the input overload-induced distortion and timing jitter (Jia Xu & Zhenghao Lu, 2011).

Typically, the extension of dynamic range is achieved by varying the TIA's transimpedance in response to the input signal strength. Numerous works have been reported on extending the dynamic range of the TIA. For example, the work (Hassan & Zimmermann, 2011) reported on a monotonic transimpedance compression with high overdrive capabilities. The full input current range is divided into two regions: linear and compression. In the linear region, the amplifier responds linearly to the input current, while in the compression region the gain is reduced in a square-root law manner in response to high input currents.

The improved design for the dynamic range was suggested in (Jia Xu & Zhenghao Lu, 2011), where AGC circuit was employed in parallel with TIA by means of an adaptive shunt feedback resistor. A combination of the peak detector, level shifter and an output buffer senses the signal strength and generates the gain control signal which is applied to the gate of the adaptive feedback resistor to control its channel resistance.

A number of programmable- and variable-gain CMOS TIA have been reported for different applications. The approaches, however, are dominated by the classical SFB TIA (Chen et al., 2005; Dash et al., 2013; Royo et al., 2016), modifications with current-mode feed-forward gain (Chen et al., 2005) or fast feed-forward architectures (Monsurro et al., 2010). In the former cases, the adjustable feedback resistance R_{F} is typically used to control the gain (Yiling Zhang et al., 2008). Such approaches often do need special care in addressing the stability issues. Specifically, as the transimpedance gain varies, it may become difficult to maintain a fixed relative position of the unity-gain frequency with respect to the non-dominant pole (Chen et al., 2005) and one ends up in a sub-optimal design.

Obviously, the reported approaches will possess the very same drawbacks as their constant-gain versions such as gain-bandwidth, noise-power trade-offs, and input capacitance isolation in SFB TIA as well as increased noise levels for fast feed-forward designs. An implementation of the programmable gain using a variable feedback resistor by adding a PMOS functioning in the linear mode in parallel with constant R_{F} may also negatively affect the noise performance of the amplifier (Manasreh, 2017). Finally, these simple strategies with a single adjustable parameter often tend to result in suboptimal amplifier configurations as one tuning knob may be insufficient in practice to adjust both the high- and low-frequency behavior of the circuit.

Some works also employed the current mode RGC amplifier as the feed-forward gain element with the feedback resistor used to implement variable-gain (Chen et al., 2004; Chen et al., 2005). The works represent an early attempt to obtain the constant-bandwidth variable-gain TIA using a single control (namely R_{F}) and low input resistance due to CG input buffers. Even though promising results have been reported for the gain between 0.3 kΩ and 1.0 kΩ, complete gain-bandwidth independence was not achieved due to a single available tuning knob. Moreover, the scalability of the technique for a larger range of gains is still questionable.

The issue with a single control value was addressed by the three-stage digital inverter-based variable-gain TIA proposed in (Sanz et al., 2007) with a second stage local feedback loop and global shunt-feedback. The design employs double control with both feedback loops implemented using NMOS transistors operating in the linear region. The gate terminal of these transistors was connected to a variable voltage which is used to control the overall transimpedance gain without degrading the bandwidth and the stability of the amplifier. The authors also emphasized that special care shall be taken to ensure the stability of the system which is directly related to the open-loop gain of the amplifier. The authors employed diode-connected transistors added to the first and third stages of the amplifier to keep the configuration stable. In their later works (Royo et al., 2017; Royo et al., 2016) the same group reported a fully-differential SFB TIA with controllable transimpedance for use in RF overlay downstream communication systems in the former case and for capacitance sensing in MEMS accelerometers in the latter case. The proposed TIA consisted of two cascaded differential pairs with a double control of both the feedback resistance and the open-loop gain. The design employed the feedback resistor R_{F} with the transimpedance adjusted to maintain the constant output average power. A linear behavior for all the input ranges was shown with the open-loop gain controlled by a variable load resistor in the first differential pair. In order to implement a variable feedback resistor with maximum linearity, the authors in (Royo et al., 2016) suggested an implementation with a parallel combination of the resistor and a digitally controlled PMOS transistor array (6-bit binary

scaled to achieve a 18 dBΩ range with 0.5 dBΩ steps). According to the authors, this allows to maximize the overdrive voltage with the transistors operating in the ohmic region and the linearity of the TIA is improved while the dynamic range is maximized. A similar implementation is also suggested for the variable load resistor in the first differential pair to control the open-loop gain. Note that both works (Royo et al., 2016; Sanz et al., 2007) employed a double control scheme to obtain constant bandwidth configurations.

An interesting approach for programmable-gain TIA was suggested in (Dash et al., 2013) with the push-pull inverter. Here the bandwidth of the amplifier was controlled by adjusting the input resistance of the inverter stage. The latter was implemented using a binary-weighted PMOS array to control the overall conductance and transconductance of the inverter. As the application of the authors required the gain to be maintained while the bandwidth is adjusted, a tunable feedback resistance bank is also employed. The implementation is based on MOSFETs used as switches which, according to (Dash et al., 2013), suffer less from process variation when compared to NMOS operating in the triode mode. The mentioned modifications are applied both to the front-end TIA as well as to the three-stage post-amplifier.

A variable-gain RGC TIA based only on active devices (no passive components) was proposed in (Monsurro et al., 2010) targeting ultrasound applications, where the variable gain is used to equalize the amplitude of the echoes. A classical voltage amplifier (push-pull inverter input stage and two CS stages with common feedback resistor) were employed by (Aznar et al., 2009) to implement a form of logarithmic compression to increase the dynamic range and to prevent the amplifier from saturation at high input currents.

An interesting variable-gain approach was reported in (Ma et al., 2018), where a diode-connected current mirror was replaced with the one which utilizes CG structure to input the current. Here again, a double control was employed, where both the load resistance and the current-mirror ratio are digitally controlled. The reported design achieved a gain larger than 100 dBΩ with the noise current density as low as 1.5 pA/$\sqrt{\text{Hz}}$ while dissipating 8 mW from 3.3 V power supply. Unfortunately, these results were achieved for the bandwidth of only 50 MHz and therefore can be hardly compared to the envisioned GHz-level OTDR application.

1.2.2. Comparison Methodology

A relatively large number of the design solutions for CMOS TIAs have been reported in the literature with each approach targeting an application-specific trade-off of the main circuit parameters. A basis for the performance comparison needs to be selected which shall serve as a unified and a clear measure for relative positioning of the numerous designs reported. This measure shall also support our

decision on which of the suggested designs shall be adopted as a basis for intended application. For example, while optical communications do not consider the linearity of the amplifier as a crucial performance measure, this may become important for non-optical applications such as magnetic resonance imaging. Even though a tabular report on the major circuit characteristics is almost always provided by the authors, the selection of the competitors is usually limited to 8 or 10 alternative solutions targeting similar application areas. Moreover, a tabular specification of the main TIA parameters often results in a mixed or an unclear impression on the superiority of the proposed scheme based on one or more key parameters from the set. Unfortunately, some of the parameters important for OTDR applications may not be reported in the most cited works on amplifier designs for optical data communications as these parameters may have a lower priority when compared to predominantly used gain, bandwidth and noise.

Similarly to some of the previous works, we try to address a problem of a unified performance metric by introducing a so-called FOM, which can be used, at least to some extent, as a single criterion for the TIA's performance assessment in selecting the best candidate for the target OTDR application. Clearly, the main requirement for this performance measure is that it should provide a fair balance for the most common TIA measures such as the amplifier's bandwidth, transimpedance gain, noise, power consumption, etc. In order to compare already known approaches as well as to position the our proposed design among the similar works, the following FOM is introduced:

$$FOM = \frac{\sqrt{BW\,[\mathrm{GHz}]}R_{\mathrm{T}}\,[\Omega]\,C_{\mathrm{T}}\,[\mathrm{pF}]}{Noise\left[\mathrm{pA}/\sqrt{\mathrm{Hz}}\right]P[\mathrm{mW}]}. \tag{1.39}$$

In the expression above P is the power in mW, C_{T} is the total input capacitance in pF, BW is the bandwidth of the TIA in GHz and $Noise$ is the input-referred noise current spectral density in pA/$\sqrt{\mathrm{Hz}}$. Note that the FOM has a physical dimensionality, but we will not use that in the bulk of the text to make the discussion easier to follow. Similar metric was recently suggested in (Hosseinisharif et al., 2020):

$$FOM = \frac{BW\,[\mathrm{GHz}]\,R_{\mathrm{T}}\,[\Omega]\,C_{\mathrm{T}}\,[\mathrm{pF}]}{Noise\left[\mathrm{pA}/\sqrt{\mathrm{Hz}}\right]P[\mathrm{mW}]}. \tag{1.40}$$

The difference is that we suggest to take a square root from the bandwidth. This makes the expression consistent, because in the denominator we have noise current spectral density measured in $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ and the final expression preserves the frequency unit in Hz.

A more consistent alternative was suggested in the works of Atef (e.g. see (Atef & Abd-elrahman, 2014):

$$FOM = \frac{BW\,[\mathrm{GHz}]\,R_{\mathrm{T}}\,[\Omega]\,C_{\mathrm{T}}\,[\mathrm{pF}]}{Noise_{\mathrm{RMS}}\,[\mu\mathrm{A}]\,P[\mathrm{mW}]}. \tag{1.41}$$

Here the author considers the RMS noise current instead of the spectral noise density as proposed by us. However, the RMS noise current is itself coupled to the bandwidth and the current noise spectral density, so using both the bandwidth and the total RMS current may be misleading and therefore bias the ranking towards designs with larger gain-bandwidth products. By taking the square root of bandwidth we penalize high-speed TIAs as those often prioritize gain-bandwidth products (e.g. TIAs designed for 40 Gbps networks) over noise. This is especially important as we do not have such a high-frequency scenario where wide bandwidth of several tens of GHz would become critically important and we want to emphasize the importance of the noise performance for envisioned OTDR applications. If one compares the best results from our suggested metric with and without square root of the bandwidth (both expressions would use spectral density in denominator), although the general ranking is somehow similar, the latter FOM selects as the best design not the capacitive feedback TIA from Shahdoost, but the older work (Oh & Park, 2007) due to its large gain-bandwidth product. However, this design cannot be considered as a good starting point for our application as it shows both relatively large power consumption and noise and it is unclear where intended low noise values can be obtained with this design by trading-off the gain-bandwidth product.

Although some alternative approaches have been suggested in the literature, they have their own limitations. For example, simpler FOMs expressions have been also suggested. The works (Jin & Hsu, 2006; Ma et al., 2018; Zohoori et al., 2019b) suggest the following metric:

$$FOM = \frac{BW\,[\mathrm{GHz}]\,R_{\mathrm{T}}\,[\Omega]}{P[\mathrm{mW}]}. \tag{1.42}$$

Such a metric would set to the top relatively noisy results reported by (Oh & Park, 2007) and (Dash et al., 2013) as it completely ignores the noise current and the ability of the amplifier to operate with large input capacitances. Differently, our proposed FOM penalizes TIA designs intended to operate with smaller input capacitances and those which have large noise currents. Thus, our proposed metric will down-rank recently reported high-speed CMOS TIA specifically designed for very latest optical transmission networks due to typically small capacitances used there. This, however, is as intended penalty, because the ability of our design to handle higher input capacitance is an important OTDR requirement.

Another interesting option is to penalize design with the transit frequency f_{T} in order to include the technology scaling as suggested in (Atef & Zimmermann, 2013; Salhi et al., 2019). Then the FOM value can be computed, for example, as following:

$$FOM = \frac{BW\,[\mathrm{GHz}]\,R_{\mathrm{T}}\,[\Omega]\,C_{\mathrm{T}}\,[\mathrm{pF}]}{Noise_{\mathrm{RMS}}\,[\mu\mathrm{A}]\,P[\mathrm{mW}]f_{\mathrm{T}}\,[\mathrm{GHz}]}. \tag{1.43}$$

This option would allow, at least in theory, select designs which come closer to the boundaries imposed by the given technologies rather than prefer designs demonstrated using newer processes. Unfortunately, in practice, the value of f_{T} is almost never directly reported by the authors and, if used, would limit the FOM analysis to a rather small set of papers or one should best guess based on the node size reported in the work.

Differently, one may not include the PD's capacitance and the noise current to the metric, but explicitly penalize the area of the design Szilagyi et al., (2014):

$$FOM = \frac{BW\,[\mathrm{GHz}]\,R_{\mathrm{T}}\,[\Omega]}{A[\mathrm{mm}^2]P[\mathrm{mW}]}. \tag{1.44}$$

However, we would like to avoid penalizing the area due to several reasons. First of all, not every work explicitly reports the design area or makes a clear separation between the TIA front-end and the rest of the circuit. Secondly, the area may be not a good indicator, because not all research works in academia try to minimize the area of the final circuit, since often the major objective is to improve the core TIA characteristics such as gain, bandwidth and noise. Finally, the designs reported in research papers may serve the purpose of proving novel design concepts and may have not the quality level of the industrial products with all auxiliary elements included.

The suggested FOM does not include explicitly penalty terms due to non-linearity or ripple in the pass-band leaving these important OTDR parameters beyond the suggested performance indicator. This is also partially caused by the fact that most of the recent works do not provide quantitative measures on these parameters and only indirect qualitative claims can be done with some caution based on the visual inspection of the reported results. The suggested FOM includes the power consumption and does not consider supply voltage separately. The metric can slightly penalize the circuits which operate at lower supply voltages, as they require additional measures to cope with voltage headroom issues. On the other hand, the proposed measure considers the reduction in power achieved by supply scaling as well as the return-on-driving current and overall driving strength of the circuit (Wilson, 2014).

If the works do not specify the value of C_{D}, a default value of 0.5 pF is used for the FOM calculations. We consider this to be a feasible assumption, because

the values in practice are between 0.2 pF and 0.6 pF for external photodiodes. For most of the works, it may be unclear whether the reported C_{D} is a true PD capacitance or a combined value including the parasitic capacitance such as the one due to ESD protection diode and pad[5]. Recall that much better gain and bandwidth results can be obtained with small values of C_{IN} and one should be careful for the performance metrics in cases when such default value is assumed for calculations.

1.2.3. Previously Published Results

The summary of the performance of the selected TIA as reported in the original works is shown in Table 1.1. When only a total input noise current is specified by the authors, the noise density is calculated using the provided bandwidth values. In some cases, the authors either do not specify the value of the C_{T} or specify C_{D} only and then, either of them is taken. Sometimes the power consumption cannot be clearly separated between the amplifier front-end and the rest of the circuit including power-hungry buffers. Bearing all this in mind, any combined performance measure such as FOM shall be only considered as a rough indicator and as an approximation of ever evading unified performance metric. For the table, only TIAs with bandwidth of at least several GHz were selected and the number of interesting low-frequency TIA such as those for MEMS or biomedical applications (Salvia et al., 2009) are not shown.

The discussion shall probably start with the series of works of Toumazou and Park dating back to the 90s (Toumazou & Park, 1996), where the authors developed a CG TIA with an additional feedback resistor from the output of the gain stage to the drain of the input stage transistor. This feedback resistor gives an additional tuning knob to control the dominant pole of the feedback amplifier. Differently from a classical case of returning the feedback to the drain of the input transistor, this new concept did not result in the reduction of the bandwidth. Later, in (Park & Toumazou 1997; Park & Toumazou, 1998) the authors addressed the bandwidth problem by suggesting the topology currently known as the RGC. The final amplifier employed RGC as an input stage with the subsequent voltage follower and again the feedback resistor to the drain of the input transistor. The demonstrated TIA outperformed the equivalent CG solution (both with feedback resistors and gain stages) in terms of the power consumption, gain and noise. Unfortunately, the original work (Park & Toumazou, 1998) does not specify the value of the input capacitance for which the simulation was performed and the value 0.32 pF was assumed. The original work of Toumazou implements something which is known as a current-mode TIA and this was elaborated further in (Booyoung Choi et al., 2008).

[5]The parasitics due to ESD protection and pads may be as high as 0.5 pF (Park et al., 2007).

Table 1.1. Performance of some reported TIAs

Work/Year	Process (CMOS)	C_{T} (pF)	R_{T} (dBΩ)	$BW_{-3\mathrm{dB}}$ (GHz)	Power/V_{DD} (mW, V)	Avg. in.-ref. noise (pA/$\sqrt{\mathrm{Hz}}$)	FOM	Topology
Park & Toumazou, (1998)	0.6 µm	0.32	61	3.5	135	4.2	1.18	RGC with voltage follower and feedback resistor
Mohan et al., (2000)	0.5 µm	0.6	58.1 / 64.1	1.2	225 @ 3.3V	17.3	0.27	differential, with CG input
Razavi, (2000)	0.6 µm		78.8	0.55	30 @ 3.0V	4.5	23.92	capacitive-feedback
Beaudoin & El-Gamal, (2002)	0.18 µm	0.2	58.7	2.6	47 @ 1.8V	13	0.45	SFB TIA with broadband matching network
Yong-Hun Oh & Sang-Gug Lee, (2004)	0.35 µm	0.6	68	1.73	50.0 @ 3.3 V	3.3	12.01	broadband cascode topology with modified inductance enhancement shunt peaking
Wu et al., (2005)	0.18 µm	0.25	61	7.2	70.2 @ 1.8V	8.2	1.31	inverter TIA with multiple inductive series-peaking, M-derived matching for input/output
Jin & Hsu, (2008a)	0.18 µm	0.05	51	30.5	60.1 @ 1.8 V	55.7	0.03	four cascaded CS stages with π-type inductor peaking
Li et al., (2006)	0.35 µm	0.6	51	6	49.5 @ 3.3 V	21	0.50	RGC input stage with shunt current feedback and inductive series peaking
Oh & Park, (2007)	0.18 µm	1.0	96	4.7	72 @ 1.8V	25	75.99	differential, advanced CG input stage, CS voltage gain stage, DC canc. f_{T} doubler
Park et al., (2007)	0.18 µm	2.0	64	2.1	50 @ 1.8V	33.2	2.76	differential, CG input stage, CS voltage gain (2x) stage
Chao-Yung Wang et al., (2007)	0.18 µm	0.15	59	8.6	18.0 @ 1.8 V	25	0.87	two-stage with pre-amplifier and post-amplifier shunt and series inductive peaking
Jin & Hsu, (2008b)	0.18 µm	0.45	75.0	7.2	91.8 @ 1.8 V			six cascaded CS stages with π-type inductor peaking
Shammugasamy & Zulkifli, (2008)	0.18 µm	0.2	62	8.1	70 @ 1.8/2.2 V	16.1	0.64	fully balanced differential with RGC input and shunt feedback/Cherry-Hooper stages and series inductive peaking. AGC module.
Aflatouni & Hashemi, (2009)	0.13 µm	0.37	57	8	1.8/10.9 @ 1.2V	30	16.68	differential RGC with combined shunt/gate inductor peaking
Bashiri et al., (2010)	65 nm	0.2	46.7	21.6	39.9 @ 1.2 V	30.0	0.17	modified RGC with local feedback with inductive peaking and series inductance
Hammoudi & Mokhtar, (2010)	0.35 µm	0.4	54.5	2.75	53.5 @ 3.3V	12.76	0.51	3x cascaded stages push-pull inverter with PMOS feedback
Han et al., (2010)	0.18 µm		61.23	5.12	18.4 @ 1.8V	11.4	6.21	RGC input stage, CS-based post-amplifier with capacitive degeneration and active inductor peaking
Momeni et al., (2010)	0.13 µm	0.25	62	6.0	98 @ 2.0V	20	0.39	2x parallel identical resistive SFB TIA
Ngo et al., (2010)	0.13 µm	0.3	50	7.5	4.1	102	0.62	RGC with broadband matching network
Atef & Zimmermann, (2012)	40 nm	0.45	47	8.0	2 @ 1.1V	23	6.18	inverter with active CD feedback, with single-ended to differential
Liu et al., (2012)	0.5 µm		57.6	1.04	73.4 @ 3.3V	18.33	0.29	RGC, CS voltage gain stage with resistive feedback, STDC.

End of Table 1.1

Work/Year	Process (CMOS)	C_{T} (pF)	R_{T} (dBΩ)	$BW_{-3\mathrm{dB}}$ (GHz)	Power/V_{DD} (mW, V)	Avg. in.-ref. noise (pA/$\sqrt{\mathrm{Hz}}$)	FOM	Topology
Yu et al., (2012)	0.13 µm	0.25	82.3	1.8	118 @	0.8	46.30	Input CS-based SFB state, level shifting stage and source follower, DC restore circuit
Dash et al., (2013)	65 nm	0.1	75.1	7.14	5.35	14.4	19.73	variable-gain with push-pull inverter PMOS array and feedback resistor bank
Escid et al., (2013)	0.18 µm		53	9.28		36.12	-	5x stages push-pull inverter with series inductor peaking and NMOS feedback
Atef & Abd-elrahman, (2014)	0.13 µm	2.0	76.8	1.6	47.3 @ 1.8V	26.5	13.96	SFB CS-based with active inductive peaking with post amplifier
Atef, (2014)	0.13 µm	2.0	64.5	1.0	3.78 @ 1.8 V	16	55.52	CS with shunt feedback resistor and current mirror load
Shahdoost et al., (2014)	0.18 µm		75.5	1.62	26.3 @ 2.2V	3.18	45.32	capacitive-feedback, DC current elimination
Szilagyi et al., (2014)	28 nm		43	22	2.0/4.2 @ 1.0V	53	3.12	RGC with 2-stage feedback amplifier (CG + CS), active inductor, Cherry-Hooper feedback resistor
Abd-elrahman et al., (2015)	0.13 µm	2.0	61.6	2.0	3.0 @ 1.5V	$>$12.4	91.41	CS/CG cascode (current reuse) with active inductor
Liu et al., (2015)	0.18 µm		87.8	1.4	8.1 @ 1.8V			3x stages push-pull inverter with series inductor peaking and AGC
Abd-elrahman et al., (2016)	0.13 µm	0.2	56.65	7.0	1.95 @ 1.5V	7.5	24.60	CS-based SFB with active cascode
Shahdoost et al., (2016)	0.13 µm		76	1.76	13.7 @ 1.5V	2.67	114.41	capacitive-feedback, DC current elimination
Salhi et al., (2017)	0.18 µm		50.8	7.9	7.2 @ 1.8V	7.7	8.79	push-pull inverter with inductive peaking and NMOS in feedback
Zohoori & Dolatshahi, (2018)	90 nm	0.2	53.5	3.5	1.28 @ 1.0V	16.8	8.23	push-pull inverter with two cascode transistors, 2nd stage CS-based with active inductor
Salhi et al., (2019)	0.13 µm	0.15	50	18	5.3 @ 1.2V	15	2.51	RGC-TIA with elliptic filter approximation bandwidth extension with bond wire as inductance
Zohoori et al., (2019a)	0.18 µm	0.5	42.24	1.96	0.97 @ 1.5V	11.7	7.98	push-pull inverter with two diode-connected transistors at input and active inductor at output
Zohoori et al., (2019b)	90 nm	0.2	40.6	4	0.274 @ 1V	13.2	11.85	modified RGC with booster
Hosseinisharif et al., (2020)	90 nm	0.25	40	6.4	1.6 @ 1.2V	25	1.58	RGC input with cascode push-pull booster and active inductor load
Soltanisarvestani et al., (2020)	90 nm	0.2	50.5	7.3	1.0 @ 1.2V	13.7	13.21	RGC input with cascode CS booster 2nd stage CS-based with active inductor
Parapari et al., (2020)	0.18 µm	0.65	68.8	5.5	18 @ 1.8V	19	12.28	differential shunt-shunt feedback with RGC input
Saffari et al., (2020)	90 nm	0.5	40.6	3.7	1.3 @ 1.2V	25.3	3.13	3-stage, RGC input, level shifer and CS base stage
Dehkordi et al., (2021)	90 nm	0.25	54.5	1.7	2.0 @ 1.0V	12.6	6.89	active feed-forward network with current mirrors and active inductors

Recently extensions to the classical RGC scheme were proposed where a cascode transistor was inserted to the classical CS-based booster amplifier to further increase the gain (and, therefore, decrease the input resistance of the amplifier) (Soltanisarvestani et al., 2020). Other interesting extensions include the capacitive neutralization technique (Martinez-Castillo et al., 2002), combination of series inductive peaking and local/global feedback loops for bandwidth extension (Rani & Dhaka, 2014) and the push-pull inverter used instead of standard CS booster (Atef & Zimmermann, 2012, 2013). The inverter stage in general has a higher gain than the CS stage. According to (Atef & Zimmermann, 2012), just a replacement of the CS stage with an inverter results in 28% reduction in the current consumption when compared to equivalently configured RGC TIA and also delivers 5 dB increase in the transimpedance gain. The difference between the classical RGC and inverter-based design is that RGC outputs from the drain of the CG amplifier with the CS amplifier functioning like a local feedback stage, while the new design takes the output from the inverter amplifier where the input stage operates like a local feedback stage. The inverter-based booster concept was further elaborated in (Hosseinisharif et al., 2020), where cascode transistors were added to the inverter stage to increase the gain further and an active inductor load was employed at the input stage. Note also that all the works (Atef & Zimmermann, 2012; Hosseinisharif et al., 2020; Soltanisarvestani et al., 2020)[6] have reported relatively small gains for proposed modified RGC input stages with cascode boosters.

A single-stage modified RGC was proposed in (Bashiri et al., 2010), where local feedback connecting the gate of M_1 to its drain was suggested. The approach employed the Cherry-Hooper technique to increase the bandwidth of the amplifier with an additional inductor placed in series with the resistor in the feedback path. According to the authors, this local feedback directly impacts the signal that flows from M_2 to the gate of M_1. This results in low-impedance and increases the operation frequency of M_1 which correspondingly increases the bandwidth of the TIA. The signal flowing to the gate of M_1 from M_2 sees M_1 as a CS amplifier and experiences the Miller effect of C_{gd}. Here the inductor is added to the feedback can be designed to resonate with C_{gd} to increase the bandwidth of M_1. Another important advantage of using this configuration is the improved biasing of the transistors as the conventional RGC suffers from the voltage headroom issue and the trade-off between input-referred noise, bandwidth and gain in high-speed TIA.

A set of works of Jin et al. (Jin & Hsu, 2006, 2008a,b) reported the designs based on multistage CS cascades with PIP for gain-bandwidth improvement and C_{D} of 450 fF in (Jin & Hsu, 2008b) and only 50 fF in (Jin & Hsu, 2006) cor-

[6] It is interesting to note here that the authors in recent work of (Hosseinisharif et al., 2020) did not comment on providing output from the inverter and seemed to employ conventional RGC output from the drain of the CG amplifier.

respondingly (the latter was incorporated to the TIA monolithically by the MIM capacitor in CMOS process). Furthermore, progressive bandwidth improvement with the addition of each inductor results in peaks of the gain frequency response with $N > 2$ as demonstrated in (Jin & Hsu, 2006). Extremely high target frequency of the circuit in (Jin & Hsu, 2006, 2008a) enforced the authors to consider a special layout to ensure the required circuit performance and signal integrity as the latter can suffer from the lossy Si substrate and crosstalk from adjacent interconnects. The authors adopted a grounded coplanar waveguide configuration of the transmission lines to prevent these problems. The same authors also experimentally demonstrated the linearity of phase and the group delay variation up to 26 GHz – the details, which are often missing from other reports. Detailed design tradeoffs behind the PIP approach can be found in elaborated work (Jin & Hsu, 2008a) which also provides guidelines for the optimal design of this inductive TIA configuration. The same work offers a basic noise analysis for PIP configuration which confirms that the PIP approach also decreases the in-band noise current with increased frequency. Although the design reported in (Jin & Hsu, 2006, 2008a) (no noise figures reported in (Jin & Hsu, 2008b)) showed relatively high noise values, the proposed strategy results in TIA with a performance comparable to that of amplifiers manufactured using the technologies with much higher f_{T}. Finally, even the reported power consumption was not very small, the ratio of the gain-bandwidth to the power was among the best at the time of original publication. As expected for inductive peaking with multistage configuration, there are significant flatness issues within the bandwidth.

An interesting design idea had been reported by (Aflatouni & Hashemi, 2009), where a classical RGC TIA was modified to have both the inductive shunt peaking and inductive gate peaking (see Fig. 1.17). The vertically stacked coupled inductors have been introduced by the authors to enhance the bandwidth via the creation of complex poles. Since the stacked inductors allow to reduce the area, the method introduces a relatively large coupling between both inductors and this coupling needs to be considered in the design. The authors also emphasized the stability conditions in such an advanced configuration. Even such an optimized architecture resulted in significant chip size compared to inductor-less designs (100 µm x 100 µm). Moreover, the noise numbers are also relatively high due to properties of the RGC stage, as we already discussed above, and they can be also partially explained by the increased noise contribution of the M_1 due to the presence of the gate inductor. An advantage of the approach is that the design is relatively insensitive to the quality factor of both added inductors and very thin traces were used to produce high inductance per area for further chip size reduction.

A variable-gain approach using push-pull inverter TIA was shown in (Dash et al., 2013). Even though only simulated data have been reported, the author claimed an extremely low power consumption of 0.32 mW for 0.86 GHz bandwidth

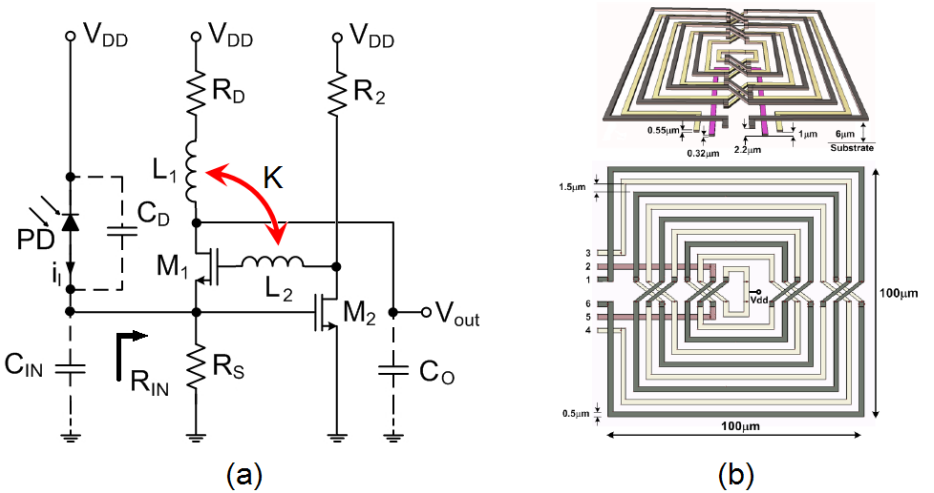

Fig. 1.17. An RGC TIA with a double peaking mechanism and mutual coupling (a) and stacked gate and drain inductor implementation (b) as suggested in (Aflatouni & Hashemi, 2009)

and noise around 8.46 pA/$\sqrt{\text{Hz}}$. The approach seems to scale up nicely up to the configuration with 13.1 GHz bandwidth along with moderate noise increase up to only 18 pA/$\sqrt{\text{Hz}}$. The variable gain was implemented as a PMOS array with a bank of feedback resistors and MOSFETs acting as binary-weighted switches. The three-stage post-amplifier and the offset compensation circuit were based on Cherry-Hooper inverter-based topology. Note, however, that the obtained results were reported for a relatively small C_{T} of just 0.1 pF.

A separate promising group of works reports TIAs using a concept of capacitive feedback. The seminal work of (Razavi, 2000) does not specify explicitly the C_{T} and also employs a 15 nH inductor in the gain stage for bandwidth extension. The results as reported in (Shahdoost et al., 2014, 2016) look extremely promising and have been mostly confirmed by experimental circuits using two different technological nodes. In terms of FOM the 0.18 µm CMOS implementation reported the value of around 45, a more advanced realization using 0.13 µm CMOS achieves the record-beating FOM of 114 - the best known result for us for application operating in the rage of several GHz. Still, there may be certain issues that could impede a direct implementation of that circuit for low-power CMOS. Here the major concern is related to the problem of a voltage headroom which can manifest itself for circuits designed to run with lower than 2.2 V supply voltage reported in his most recent work. Furthermore, none of the works specified the lower bound on C_{T} used for simulation and measurement characterization. This makes it harder to position this promising design within the results of competing works as the numbers

reported by the author may be overoptimistic and the circuit performance with realistic C_{T} may appear somehow worse. Finally, both reported designs (Shahdoost et al., 2014, 2016) resulted in significant peaking in the frequency response (around 1.3 dB in 0.18 μm design and even larger in 0.13 μm design) and the bandwidth of the design with flat bandpass may be also somewhat smaller.

Relatively simple push-pull single stage (Salhi et al., 2017) or multiple cascaded stages (Escid et al., 2013; Hammoudi & Mokhtar, 2010; Liu et al., 2015; Wu et al., 2005) TIAs have been also proposed. In some cases, a MOSFET device in the triode region was employed to optimize the noise when replacing a default resistor in the feedback path. An inductor in the feedback path was used to extend the bandwidth in (Salhi et al., 2017), while different types of series inductive peaking were also suggested in (Escid et al., 2013; Liu et al., 2015; Wu et al., 2005).

Although a very good performance was reported in (Escid et al., 2013; Salhi et al., 2017), the works do not detail the values for C_{T} used for simulation and even expected power consumption in (Escid et al., 2013). Relatively good noise figures were reported for multiple inductive-series technique in (Wu et al., 2005), where the proposed wide-band architecture consisted of the inverter gain stages with on-chip inductors deployed between them. Here the deployed inductors with the parasitic capacitances resemble a third-order LC-ladder filter to perform an impedance transformation network. Obviously, the technique also allows absorbing the PD's capacitance as a part of the impedance transformation network. The authors also claimed that the series approach manifests larger bandwidth enhancement and less sensitivity to an on-chip inductor quality factor when compared to more classical shunt-peaking techniques (Wu et al., 2005). A surprisingly good performance was shown in (Liu et al., 2015), but the work skips the exact specification of the C_{T} for which the simulation results are shown.

The authors in (Liu et al., 2012) implemented an RGC concept with a CS-based voltage amplifier and a second voltage gain stage with a dedicated feedback resistor. A single-to-differential converter with active inductor peaking was introduced to alleviate possible bandwidth degradation. Although the measurements of the manufactured circuit were demonstrated, the authors also did not specify the value of C_{T} while most of the power consumption is attributed to the output buffer.

The work (Park et al., 2007) provides one of the examples of CMOS TIA design, where the CG input stage was selected to relax the trade-off between the bandwidth and the large PD capacitance (2.0 pF for the total input capacitance including C_{D} of 1.5 pF, ESD protection pad, etc. for DVI/HDMI applications). The authors have chosen the differential design to eliminate the common-mode noises with the subsequent two-cascaded voltage-gain stages designed as conventional CS differential amplifiers with active PMOS loads. Although the authors did not specifically target low-noise design, relatively poor noise performance of the circuit may be still attributed to the CG input stage.

Right around the time, the same team also reported on a differential 12-Channel 60-Gb/s transimpedance amplifier (Oh & Park, 2007). Although the classic CG input stage already has a relatively small input impedance, according to the authors, this was still insufficient to isolate totally the input capacitance due to poor device characteristics of conventional CMOS and used RGC TIA for further performance improvement. The gain stage of TIA has been designed again as a CS amplifier with feedback resistor R_{F}, although this time a single stage was sufficient. Finally, the DC-cancellation stage was designed of f_{T} doubler type for this block to prevent reducing the total bandwidth. The reported design showed extremely good results in terms of the FOM (computed value around 76) with the improvement mainly due to both increased gain and bandwidth, while the absolute noise figures still remained relatively poor. Similarly to the design reported in (Park et al., 2007), this may be again attributed to the relatively weak noise performance of the input RGC stage. Here high gain can be partially attributed to a special implementation of the limiting amplifier using active feedback technique with negative capacitance compensation. In general, usage of f_{T} double techniques to extend the bandwidth may result in a higher value of power dissipation when compared to obtaining the same results with alternative techniques (Soltanisarvestani et al., 2020).

Even though the inductor peaking results in significant bandwidth improvement for high-speed CMOS TIAs, many works reported attempts in improving the bandwidth using inductor-less TIA configurations. For example, (Momeni et al., 2010) suggested using N identical resistive-feedback TIAs in a parallel configuration to boost the bandwidth while keeping the transimpedance gain constant. This is achieved as the C_{D} is now effectively divided between each of N parallel TIAs moving the dominant pole to a higher frequency. According to the authors, the assumption of an ideal adder would not significantly affect the results as it can be realized using common-source buffers at the output of each SFB TIA and by adding their currents through a single resistive load. Here the buffers need to have a gain of 1 and hence they can have the bandwidth much higher than the TIA itself. As the number of the parallel TIAs increases, the effective damping factor of the combined TIA decreases translating to more oscillations (i.e. ringing) in the step response of the amplifier. This overshoot in the time domain corresponds to the peaking in the frequency domain and resembles the effects of the inductive peaking technique. The difference is that while in inductive peaking the bandwidth improvement comes at the cost of additional chip area used for the inductors, in the proposed configuration the power consumption is mainly traded-off. A clear advantage of the proposed scheme is that it can be used essentially for any TIA topology. Unfortunately, a higher number of the core TIAs also results in higher input-referred noise, therefore in terms of the noise, ringing and power consumption one shall not use more than two or three amplifiers connected in parallel.

A surprisingly low noise performance for a circuit with CS-based SFB input

stage was shown in (Yu et al., 2012). In terms of our suggested FOM, the reported work demonstrates rather good performance with the value reaching 46.3. Even though rather low C_{D} value was used for simulation (250 fF) in parallel with high power consumption (118 mW) of the circuit, the authors doe not specify on the detailed mechanism to achieve such good noise performance using this classical topology. Still, this work may be seen as an example on how good performance we can achieve if we stay with the classic SFB architecture.

An interesting and relatively simple concept was suggested in (Abd-elrahman et al., 2016), where a classical CS-based SFB TIA was modified in two steps. First, a cascode CS implementation was used to increase the bandwidth and decrease the Miller capacitance. Secondly, a lateral auxiliary amplifier was introduced to improve the cascode effect by boosting the transconductance of the cascode transistor. The suggested active cascode scheme resulted in a bandwidth increase of almost 50% with a power penalty of only 0.13 mW.

A two-stage approach with both shunt and series inductive peaking was suggested in (Chao-Yung Wang et al., 2007). Here the pre-amplifier was based on a cascode amplifier with a dedicated source follower utilized for local resistive feedback. The post-amplifier is also composed of a cascode amplifier and a source follower which are used to provide the voltage gain and to serve as a buffer, respectively. For both the pre- and post-amplifier inductive shunt peaking techniques were applied to achieve sufficient bandwidth (the authors targeted 10 Gb/s data rate applications) with an additional series inductor inserted at the inter-stage.

A relatively good performance with classical broadband cascode TIA structure was reported in (Yong-Hun Oh & Sang-Gug Lee, 2004). The authors employed a special inductance enhancement shunt peaking as a load to increase the bandwidth while keeping low both noise and on-chip inductance. The authors stated that the new shunt peaking technique is applicable to broadband amplifiers with a bandwidth of 1–2 GHz, since the bandwidth can be extended with relatively little inductance by the principle of inductance amplification. The proposed technique allows amplifiers with high and yet flexible gain and wide bandwidth at the same time. Moreover, the authors in (Yong-Hun Oh & Sang-Gug Lee, 2004) claim that the proposed inductor load results in reduction of the noise generated by the input stage of the amplifier.

Some works reported on attempts to mitigate the disadvantages of passive inductors by using the active inductors (Abd-elrahman et al., 2015; Atef & Abd-elrahman, 2014; Han et al., 2010; Hosseinisharif et al., 2020; Soltanisarvestani et al., 2020; Zohoori et al., 2019a). Even though limitations on the bandwidth due to input pole have been addressed in (Atef & Abd-elrahman, 2014), the design showed relatively large noise. The input stage of the proposed amplifier was able to deliver only around 46 dBΩ, while the rest of the gain was obtained using a dedicated post amplifier formed by a single-ended voltage amplifier, single-

ended to differential converter, pre-driver and 50Ω driver. A combination of the active inductor and capacitive degeneration was reported in (Han et al., 2010) for the CS-based stage after input RGC stage. Similarly, a combination of capacitive degeneration, input matching network, input RGC stage had been suggested in (Jia Xu & Zhenghao Lu, 2011) to significantly increase the bandwidth of the amplifier. Promising bandwidth extension with moderate power consumption had been demonstrated, while moderate noise level is likely to be caused by the inherent properties of the input RGC stage. However, capacitive degeneration peaking may suffer from lower DC again (Atef & Zimmermann, 2012). The work (Abd-elrahman et al., 2015) demonstrated a current-reuse scheme with an active inductor peaking. The current-reuse scheme consisted of a cascode configuration of a classical CS-based amplifier with resistive feedback and a corresponding CG amplifier. Compared to an original cascode-only configuration, the version with active inductor demonstrated significantly increased bandwidth at the price of increased noise (Abd-elrahman et al., 2015). Interestingly, the work of (Abd-elrahman et al., 2015) demonstrates the second best result in terms FOM after the capacitive feedback TIA of Shahdoost with computed value around 91.4.

A combination of several techniques had been suggested in (Szilagyi et al., 2014) in order to implement a TIA for 30 Gb/s communication link in 28 nm 1 V CMOS process. The authors addressed the voltage headroom problem by modifying the RGC TIA to have a 2-stage feedback amplifier, where the first CG stage shifts the voltage level at the input of the amplifier closer to the supply voltage, while the second high gain CS stage increases the gain in the loop. The authors also employed the Cherry-Hooper configuration to reduce the effect of the parasitic capacitance in M_1. Finally, an active inductor is used for bandwidth enhancement. The work is an excellent example of the fact that several circuit-level modifications of the reference TIA topologies may be needed to satisfy the requirements of standard CMOS.

In spite of an overwhelmingly large number of works reported on CMOS TIA design, relatively few works discuss the effect of process variation on the performance of the target circuit. A decent exception is the series of works of Atef (Abd-elrahman et al., 2015, 2016; Atef, 2014; Atef & Abd-elrahman, 2014), Zohoori (Zohoori & Dolatshahi, 2018; Zohoori et al., 2019a) and Royo (Royo et al., 2016), where Monte Carlo simulations were performed to analyze the variations in the transimpedance gain, bandwidth and noise. For example, the work (Atef & Abd-elrahman, 2014) demonstrated that while the standard deviation of the gain can be below 1.5 dBΩ for the input-stage TIA, the standard deviation of the bandwidth was close to 160 MHz which becomes almost 10% of the nominal amplifier bandwidth. A comparison with the other results of the same group (Abd-elrahman et al., 2016) showed that there are significant differences both in gain and bandwidth sensitivity for different topologies. Unfortunately, similar information for

results from other authors is typically missing and this does not allow us to evaluate the effect of the process variations on most of the proposed designs. Also of interest are the works (Zohoori & Dolatshahi, 2018; Zohoori et al., 2019a) where the authors considered the impact of the temperature and variations in supply voltage on the power consumption, transimpedance gain and bandwidth of the amplifier.

Some attempts to use a broadband matching with classical RGC have been reported in (Beaudoin & El-Gamal, 2002; Ngo et al., 2010), where the matching network included the C_{D}, the inductance of the bond wire, and an additional on-chip inductance. The works provide good practical examples on how the bonding wire can be exploited as an element of the matching network. Since the exact value of the bonding inductance cannot be guaranteed due to process variations (typically between 0.7 and 2 nH), one may need to choose the additional inductance optimally for wider bandwidth with negligible gain peaking. Although the RGC-based approach reported in (Ngo et al., 2010) was probably responsible for a relatively large noise reported, a similar approach using SFB TIA demonstrated relatively small noise around 13 pA/$\sqrt{\mathrm{Hz}}$ in (Beaudoin & El-Gamal, 2002).

There have been rather few works that have tried to compare different designs under otherwise equal conditions. A simulation-based comparison of SFB, CG and RGC TIA was provided in (Aflatouni & Hashemi, 2009), where minimum design current was reported depending on the PD's capacitance. Although the devices were optimized for a particular application of the authors (10 Gbit/s with 8 GHz bandwidth), the simulation clearly demonstrates that the CS-based SFB TIA has the worst scaling with increasing C_{D} for high-frequency applications. At the same time, RGC TIA seems to have the lowest minimum device current from all three reference architectures.

For comparison with research works, the performance for a number of commercially available products is shown in Table 1.2. Obviously, the commercial amplifiers do not have the required flexibility and typically have significant power consumption when compared to custom designs reported in academia. LTC6561 is a four-channel multiplexed TIA with output multiplexing, AD8015 is a wideband differential output TIA and HMC799LP3E is a special TIA for optoelectronic laser sensor applications.

Table 1.2. Performance of some commercially available TIAs

Parameter	LTC6561	AD8015	HMC799LP3E
C_{T}, pF	2.0	0.2	
R_{T}, kΩ	74	10	10
$BW_{-3\mathrm{dB}}$ / Data rate, GHz	0.2	0.24	0.7
Power/V_{DD}, [mW, V]	200 @ 5V	125 @ 5V	350 @ 5V
Avg. in.-ref. noise, (pA/$\sqrt{\mathrm{Hz}}$)	4.5	3.0	5.7

If we take the developed FOM as an indicator which design look promising and shall be followed for the envisioned OTDR TIA, there are several interesting observations to be made. First, let us consider the works which reported the best FOM values as shown in Table 1.1. The largest FOM value is reported in (Shahdoost et al., 2016) for capacitive feedback TIA. Here the value of FOM reaches 114.0 with the transimpedance gain of 76 dBΩ, 1.76 GHz bandwidth and noise 2.67 pA/$\sqrt{\text{Hz}}$ while consuming 13.7 mW at 1.5 V power supply. Differently from other promising works, the superior performance of the design was also confirmed experimentally in 0.13 µm CMOS. The scalability of the design for lower cost 0.18 µm CMOS was confirmed by the very same authors in their earlier work (Shahdoost et al., 2014), where the gain of 75 dBΩ, bandwidth of 1.62 GHz, noise current density 3.18 pA/$\sqrt{\text{Hz}}$, and power consumption of 26.3 mW at 2.2 V power supply were reported while reaching FOM of 45. Both 0.13 µm and 0.18 µm designs were proposed for 2.5 Gb/s optical communication systems. Unfortunately, the author did not report an exact value of C_{T} employed in the system and the superior FOM values were obtained assuming a default C_{T} of 0.5 pF. Clearly, this assumption may render the exact performance indicator less accurate, although the difference from competing works demonstrates sufficient margin. Note that the second best result reported in (Abd-elrahman et al., 2015) delivers noise above 12 pA/$\sqrt{\text{Hz}}$ and it is unclear whether we can trade-off the noise against other design parameters such as high value of C_{T}. Due to aforementioned reasons the capacitive feedback TIA seems to be the most promising candidate for the design of the low-noise CMOS TIA targeting OTDR applications as it reports the best performance in terms of FOM which had been also confirmed by measurements.

1.3. TIA Circuits for OTDR

The OTDR is a well-established tool widely used for testing the attenuation characteristics of the optical fibers (Tateda & Horiguchi, 1989). Usually the technique is employed to characterize the faults, loss and damage along the optical fiber link, where the precise location of the faults can be detected alongside with the nature of the problem. The technique can be also used to evaluate the fluctuations of the fiber's parameters and is extremely useful for the case of optical transmission lines composed of several optical fiber cables. Moreover, the OTDR is also often used for estimating the capacity and real-time performance of optical networks (Shi et al., 2016).

The major OTDR characteristics are the ADZ and the dynamic range with an ideal OTDR instrument having zero ADZ and an infinite dynamic range. The latter can be achieved using the noiseless optical receiver with an infinite bandwidth and delta function type laser pulses (Charlamov & Navickas, 2015). In reality, due to effects such as nonlinear Kerr effect, the laser power is limited to around 1 W and delta function laser pulses cannot be used. Therefore, in order to deliver more energy and to achieve a higher SNR, the pulse width must be increased. As a result, either ADZ or dynamic range shall be sacrificed. Finally, the key OTDR design goal becomes the maximization of the SNR as a function of bandwidth. The instruments commonly used pulse widths from 5 ns to 10 μs which require the bandwidth of the optical receiver between 50 kHz and 130 MHz.

A typical OTDR instrument may contain a number of parts, or modules which provide the required functions. These modules may include the waveform generator (one or more laser diodes), a detector, a signal processing function and a display. The instrument should also provide facilities to allow connection to the fiber-under-test such as a directional coupler and a fiber connector. The block functions of a typical OTDR instrument are shown in Fig. 1.18.

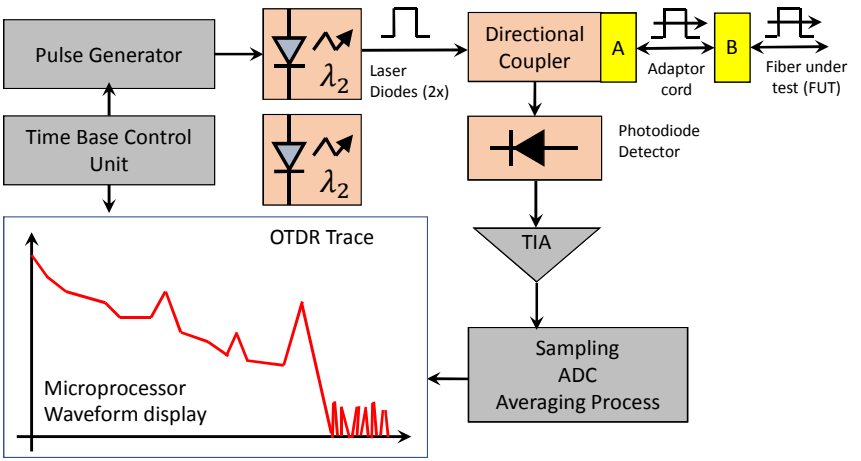

Fig. 1.18. Block functions of a typical OTDR instrument

In general, there are several OTDR techniques such as CR-OTDR, where the dynamic range performance is improved without sacrificing spatial resolution of the instrument by using the correlation property of pseudo-noise random coded signal (Kang et al., 2014). Here a pseudo-random bit sequence is used to modulate the optical pulse and the correlation between the back-scattered light and the delayed bit sequence is obtained by the cross-correlator. Furthermore, one

could employ a Photon Counting OTDR, where the APD in Geiger mode is used. When an APD is biased about its breakdown voltage, it becomes possible to detect even single photons, although further steps can be necessary for elimination of the dead zone due to charges getting trapped in the APD causing an unwanted extra avalanche.

Another interesting application of OTDR mechanism is its adoption as a temperature or stress-strain sensing technology via using, for example, Phase OTDR, Raman-assisted OTDR or FBG-based OTDR (Xia et al., 2012; Xie et al., 2018). For example, in the case of FBG-based OTDR a region of periodic variation in refractive index is inscribed in the core of the optical fiber. In this case, it is possible to control the reflection of a propagating optical signal at particular wavelengths. As the wavelength with the strongest reflectivity depends on the Bragg grating period, temperature and the mechanical strain, it can be used in temperature and strain sensing applications using a setup similar to classical OTDR as described above. Additional changes are necessary to sweep the wavelength of a tunable laser so that an OTDR measurement is done at each wavelength and an associated signal processing is employed to find the wavelength at which the strongest reflection occurred, thus determining the corresponding strain or temperature gradient.

An interesting application of temperature sensing is the health monitoring (temperature, stress/strain) of the wires in power transmission systems (Xie et al., 2018). The approach allows not only to monitor the temperature of the transmission lines, but also to detect galloping in real time while analyzing the OTDR signal in the frequency domain. The system allows to form the sensor network in the power grid which is an interesting and promising OTDR application area. A special attention had been demonstrated to the analysis of the tree-structured PONs, where all back-scattered traces add together at the terminal location, thereby making it difficult to differentiate between the branches (Yuksel et al., 2007). Interesting technical solutions have been proposed to address the problem of OTDR in tree-structured networks such as placing the dedicated switchable-reflective elements at each optical network unit location. Here the signature of the placed reflective element can be identified in the OTDR trace thus allowing a centralized method for an in-service monitoring (Yuksel et al., 2007). Such a system is able to localize and quantify several faults successively in the same branch or in different branches even if they occur at the same distance. Further modifications of the classical OTDR setup are possible such as Raman pump for the dynamic range and sensing distance extension in OTDR (Kharasov et al., 2018; Sato et al., 1992; Spirit & Blank, 1989; Yuksel et al., 2007). An interesting application of the OTDR was also shown in (Wuilpart et al., 2003), where a tunable setup was employed to determine the Raman gain spectrum of each optical link fiber. Further information on different types of OTDR systems can be found in (Charlamov, 2013).

Few TIA designs have been reported specifically addressing OTDR require-

ments. The work (Charlamov & Navickas, 2015) proposed a fully differential SFB TIA with programmable gain. A classical resistive feedback topology was chosen with design targeting the bandwidth of 130 MHz. As the design required high values of the feedback resistors R_{F} (up to 800 kΩ), it could have became susceptible to electromagnetic interference and a differential TIA structure was suggested. An additional advantage of the chosen differential design is also due to the high power supply and common-mode rejection ratios. The programmable gain was implemented using switchable feedback resistors connected in series with single-pole double-throw switches to reduce input capacitance with five resistor pairs needed to achieve the target range of gains. A fully-differential approach was taken with an additional beta-multiplier based generator for a dedicated start-up circuit to ensure stable tail current. The achieved TIA bandwidths were reported from 6 MHz at the gain of 118 dBΩ to 125 MHz at the gain of 87.25 dBΩ. The design reported by the authors is shown Fig. 1.19 with more than 30% of the topology area occupied by the feedback resistors. Unfortunately, the author did not go beyond this classical architecture and typical issues of this reference topology including lower noise performance have remained unaddressed. Furthermore, the final implementation also demonstrated some overshoot for the configuration with the largest gain.

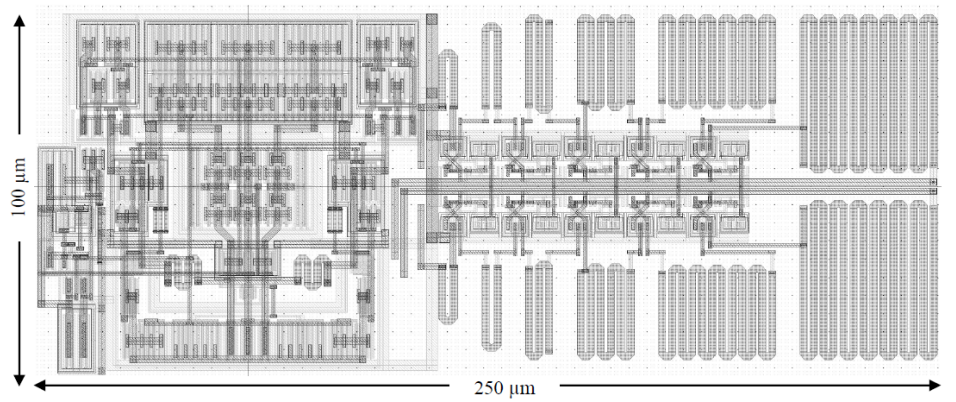

Fig. 1.19. Programmable-gain CMOS TIA for OTDR applications (Charlamov & Navickas, 2015)

Several recent works also reported integration of TIA into a complete lower performance OTDR ASICs (Yeom et al., 2019) and even use the OTDR capability directly in the optical transceiver modules (Kuznia et al., 2014). The availability of high-speed and high-density ASIC technology has made it possible to integrate all the functions required to create the OTDR measurements on a single chip and even use the OTDR capability directly in the optical transceiver modules for fiber optic BIT in avionics (Kuznia et al., 2014; Nazer et al., 2019). Here the OTDR module is

integrated into the fiber optic transceiver to fault isolate fiber optic interconnects up to several centimeter resolution (Nazer et al., 2019). Originally, a single chip integration OTDR ASIC developed by Ultra Communications Inc. was announced for higher resolution OTDR applications (Kuznia et al., 2014). The system provides the necessary clocking, timing/pattern generation (arbitrary 20-bit pattern), receiving and sampling functions needed to implement all the required functionality within a compact transceiver module and physical layer components while having dimensions of just 4.0 mm $\times$ 1.655 mm. The programmable timing circuits were able to operate up to 10 GHz with output in current-mode logic signal format and four-channel receiver/sampling circuit. The presented solution could generate pulse widths of 100 ps and sample at 100 ps resolution, which is approximately equal to the round-trip time for an optical pulse to travel 1 cm in fiber. Moreover, within the architecture, the pulse width can be easily adjusted by setting a different bit pattern while enabling both flexible and low-cost implementation of OTDR within physical layer components. According to the authors, both the offset and the gain of TIA and associated post amplifiers could be tuned appropriately for detecting small and large signals. Even though the TIA was only a minor part of the complete chip and no details on its architecture or performance characterization have been reported in the original publication of authors, the detection scheme as proposed by the authors was designed to measure only the reflective events in the optical pathways and not the Rayleigh backscattering. This fact is a potential indicator that no special requirements for the TIA performance have been set and a classical resistive feedback approach was employed. Also note that the OTDR pulse amplitude was limited so it did not saturate the linear receiver eliminating the typical OTDR issue with the dead zone.

A SOC solution for OTDR had been also demonstrated in (Shi et al., 2016). The developed circuit could be configured into several modes including high-performance mode (external modulator, expensive off-chip laser and PD) as well as low-cost mode (low power/gain with inexpensive laser and PD). The developed circuit achieved a maximum detectable fiber length of 25 km with the spatial resolution of 2.5 m, 4 m and 10 m respectively depending on the configuration. When compared to the discrete solutions on the market for the year of publication (2016), the integrated system was expected to reduce the cost by factor 100, area by factor 5 and power consumption by factor 4. The received signals due to Rayleigh backscattering were below the noise level of the system, therefore only the measurements of Fresnel reflections could have been demonstrated[7]. The work employed a two-stage TIA with common-mode feedback and corresponding amplification of 20 dB and 10 dB. The TIA is followed by a second-order low-pass filter with bi-quad ar-

[7]Fresnel reflected light intensity is greater than Rayleigh backscattered light by about 3 or 4 orders of magnitude (Tateda & Horiguchi, 1989).

chitecture and 20-40 dBΩ tunable gain (step size of 10 dBΩ). Furthermore, an inverse Thomas-Tow bi-quad technique and DC offset cancellation are employed for low-noise and offset compensation. Finally, the authors have placed a programmable gain amplifier between the filter and the output buffer to provide a final amplification for an output scale of 30 dBΩ with a 1 dBΩ step.

Recently, yet another ASIC implementation of the OTDR module had been demonstrated in (Yeom et al., 2019). The OTDR ASIC was implemented using 350 nm CMOS process and occupied the area of 5 mm by 4 mm while operating from 3.3 V power supply. The authors employed a classical resistive feedback TIA where an additional feedback capacitor C_{F} was added in parallel with the feedback resistor R_{F} to improve the stability. The programmable gain was achieved by varying R_{F} with resistor multiplexing. The core voltage amplifier was designed as a 2-stage OP-Amp due to simultaneous requirements on high bandwidth and wide output swing. The authors also implemented a sample & hold amplifier to decouple the TIA and ADC circuits as the latter may be seen as a large load capacitance that may affect the performance of TIA.

An implementation of the CR-OTDR has been demonstrated in (Kang et al., 2014), where again a classical resistive feedback TIA with an additional feedback capacitor C_{F} was employed. The intended spatial resolution of the instrument was set to five meters, hence the required bandwidth of around 20 MHz can be achieved with trivial TIA designs.

1.4. Requirements Analysis and Technical Specification

In order to properly evaluate the suitability of the reported TIA topologies for the intended application, a preliminary specification for the CMOS TIA shall be developed. Based on the analysis of the performance of state-of-the-art CMOS TIA and OTDR systems in previous sections as well as supported by the discussion with companies that develop commercial OTDR systems, we can proceed with setting up a set of specifications in this section. Due to commercial and performance reasons the specification is provided for classical OTDR systems. The pros and cons of alternative OTDR techniques can be found, e.g. in (Charlamov, 2013).

The performance of a standard optical reflectometer is typically described in terms of two key parameters: attenuation dead zone (ADZ) and dynamic range (DR), where an ideal OTDR shall have correspondingly a zero ADZ and an infinite DR. While ADZ depends mainly on the injected pulse width and the bandwidth of the optical receiver, the DR is a measure of device sensitivity and depends not only on the pulse width and bandwidth, but additionally on the power of the laser

pulse and the gain of the optical receiver. Therefore, any decent design shall target high DR for the given value of ADZ. First, we start with computing the requirement for the bandwidth following the methodology similar to the one proposed in (Charlamov, 2013). The refractive index n is defined as the ratio of the speed of light in vacuum c to its velocity in the medium v:

$$n = \frac{c}{v}. \tag{1.45}$$

In our case we take $n = 1.486$ which numerically means that in 1 ns the light in fiber propagates for 0.2 m. The specification is based on the requirement not to exceed the double length of the pulse T_0, when the Fresnel reflection coefficient is -45 dB. The reflectometer counts for the both forward and backward path, therefore we get that 10 ns pulse is equivalent to approximately one meter. Then the pulse duration in meters becomes 0.4/2 = 0.2 meters and for the given light speed in the fiber we get the pulse duration around 1 ns. Next we need to compute the corresponding reflection amplitude. The reflected power can be written as:

$$P_{\text{refl}} = P_0 \cdot R_{\text{L}}, \tag{1.46}$$

where P_0 is the pulse power and R_{L} is the reflection coefficient. The power of the back-scattered light P_{bsc} depends on the back-scattering coefficient Bs, P_0 as well as the pulse duration T_0:

$$P_{\text{bsc}} = Bs \cdot P_0 \cdot T_0. \tag{1.47}$$

If we represent the pulse power in dB w.r.t. 1 mW and time in 1 ns, then the reflection amplitude r becomes (all in dB):

$$r = \frac{R_{\text{L}} - Bs - T_0}{2} \quad [dB]\,. \tag{1.48}$$

The expression above is formulated in logarithm base 10 scale, therefore if one wants to get to reflectometer scale logarithm base 5, the computed value r shall be divided by 2. The computations are rather straightforward. For example, for the 1310 nm fiber and pulse length T_0 equal to 100 ns we get Bs equal -79 dB, R_{L} is set to -45 dB by measurement standard specification, while T_0 equal to 100 ns, when transformed to 1 ns scale in dB results in 20 dB (Charlamov, 2013). Then (all in dB):

$$r = \frac{-45 + 79 - 20}{2} = 7 \quad [dB]\,. \tag{1.49}$$

With the methodology above we are able to determine r for particular reflection R_{L} and given duration of the pulse T_0. The dead zone is the sum of the pulse width T_0 and the attenuation (discharge) time t. Although the pulse duration is given or

can be seen as a tuning parameter, the decay time shall be computed. The rest of the calculations are based on the assumption that the pulse propagation takes place in the first-order circuit which can be completely described by its time constant τ. From the assumption on system being first-order, a simple relationship between the bandwidth and the time constant is established:

$$BW_{-3\mathrm{dB}} = \frac{1}{2\pi\tau}. \tag{1.50}$$

For the first order low-pass filter the corner frequency ω_c is the same as the -3 dB frequency. However, what we are looking for here is not the conventional -3 dB bandwidth, but a so-called equivalent noise bandwidth. This value is defined as the bandwidth of a brick-wall filter which produces the same integrated noise power as a real filter. This value is also sometimes referred to the noise bandwidth or the effective noise bandwidth. If we take the transfer function of the filter $H\left(j\omega\right)$, such bandwidth becomes in general case:

$$BW_{\mathrm{ENBW}} = \int_0^\infty \left| \frac{H\left(\mathrm{j}\omega\right)}{H_{\max}} \right|^2 d\omega, \tag{1.51}$$

where $H_{\max}$ is the maximum value of $H\left(\mathrm{j}\omega\right)$ or, correspondingly, magnitude of brick-wall filter in ideal pass-band. In other words, BW_{ENBW} is defined as the frequency at which the brick-wall filter has the same integrated noise power as the first-order system under analysis. For our assumed first-order system it can be shown that:

$$BW_{\mathrm{ENBW}} = \frac{\pi}{2} BW_{-3\mathrm{dB}} \approx 1.57 BW_{-3\mathrm{dB}} = \frac{1}{4\tau}. \tag{1.52}$$

Finally, the discharge time can be computed from the assumption of a simple first-order RC circuit, where the voltage drop can be written in a simple exponential form:

$$V = V_0 \mathrm{e}^{\frac{-t}{\tau}}. \tag{1.53}$$

Then the ratio between the initial and actual voltages at time t becomes:

$$r = \frac{V_0}{V} = \frac{V_0}{V_0 \mathrm{e}^{\frac{-t}{\tau}}} = \mathrm{e}^{\frac{t}{\tau}}. \tag{1.54}$$

One may re-arrange the expression above to get a time constant τ:

$$\tau = \frac{t}{\ln\left(10^{\frac{r-0.5}{5}}\right)} \approx \frac{t}{0.46}\left(r - 0.5\right). \tag{1.55}$$

Note that we have subtracted the value 0.5 (in dB) from the r due to specifics of the pulse measurement process. Putting all together we get the ADZ in meters as:

$$ADZ = \frac{c}{2n}(T_0 + t). \tag{1.56}$$

The methodology above needs a specification of both the T_0 of the pulse and the bandwidth for the dead zone estimation. For example, for T_0 = 5 ns, BW_{ENBW} of 100 MHz we get r equal to 13.5, τ becomes 2.5 ns and the discharge time t becomes 14.9 ns. The total dead zone time becomes close to 19.9 ns with the ADZ length being approximately 2.01 m. These results are close to the calculations reported by (Charlamov, 2013). The dependencies of ADZ on the bandwidth BW_{ENBW} for several representative values of T_0 and the reflection R_{L} = −45 dB are shown in Fig. 1.20. Obviously, smaller T_0 allows us to achieve smaller ADZ, where the saturation level is reached much earlier for OTDR equipment with larger pulse width. It is also educative to see that after some critical value the further increase in bandwidth does not provide any improvement in terms of ADZ as it becomes limited by the value of T_0.

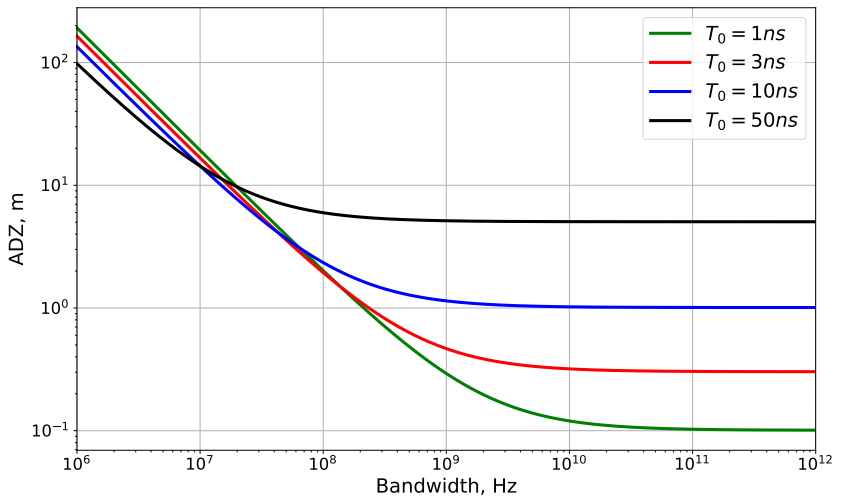

Fig. 1.20. ADZ dependency on the bandwidth BW_{ENBW} for different values of T_0 and fixed R_{L} = −45 dB

A different perspective to the same process can be seen in Fig. 1.21, where the dependency of ADZ on the pulse width T_0 is plotted for several representative values of the bandwidth (between 100 MHz and 1 GHz) and reflection R_{L} = −45 dB. What is interesting here is that there seems to be an optimum value of the pulse width for the given bandwidth, although further investigation at this point may

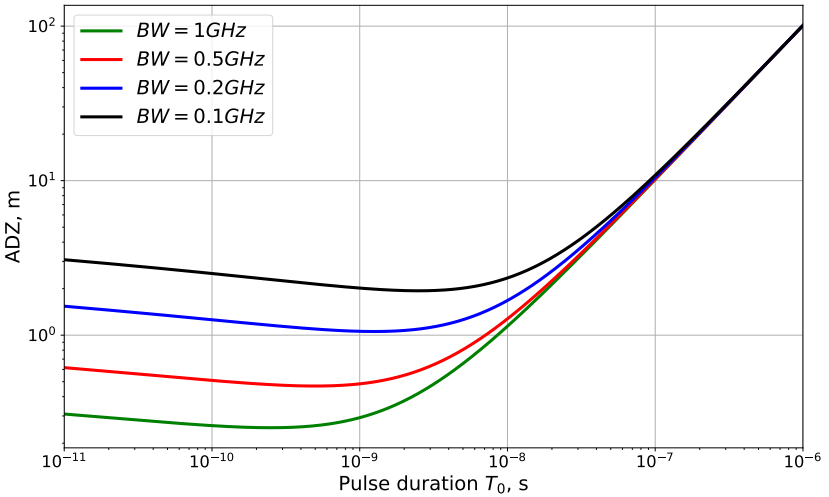

Fig. 1.21. ADZ dependency on the pulse width T_0 for different values of BW_{ENBW} and fixed $R_{\mathrm{L}} = -45$ dB

be necessary as this optimum may be an artifact due to some assumptions in the derivation above (e.g., first-order model assumption, etc.). With this information in mind we are able to derive the requirements on the bandwidth for the target TIA. As our objective we can consider high-performance and high-resolution OTDR instruments from LUCIOL INSTRUMENTS: models LOR-200 and LOR-220 (see (LUCIOL, 2021, 2022) for further technical details). Note that the latter model is a model explicitly designed for demanding aviation, defense, transportation and oil applications and its specifications far exceed that of devices commonly used for conventional optical networks. If we target the superior performance of LOR-220, we shall consider pulses with T_0 equal to 1 ns. The attenuation dead zone for LOR-220 is specified to 0.4 meters. If we take a bit tighter ADZ of 0.3 m to compensate possible errors in modeling, we end up with the bandwidth close to 1 GHz which we can take as the requirement for our optical receiver front-end. Note that if we would stay with the amplifier made from discrete components, our bandwidth would be likely limited to around 100 MHz. Fig. 1.21 provides a clear estimate which ADZ one could expect for such a design and independently on T_0 the dead zone will be limited to several meters. For comparison, in the case of optical communication systems, the bandwidth of the corresponding TIA is usually optimized to be between 60% and 80% of the desired bit-rate due to the design trade-off between the noise and ISI performance. Differently, in the present OTDR application, the bandwidth shall be derived from the used pulse width and the requirement for the attenuation dead zone while taking into account the equivalent noise bandwidth.

The requirement for the gain can be only partially computed from the specification for the DR alone. For the case of OTDR single measurement (no averaging), we get the dynamic range from SNR as:

$$DR = 5 \log \left(\frac{S}{P_{\mathrm{NEP}}} \right), \tag{1.57}$$

where S is a maximum signal level at the output of a TIA and P_{NEP} is the noise equivalent power. Although only one DR requirement is known (50 dB), we need to compute two of the other key TIA parameters: input-referred noise current density and the gain of the amplifier. It had been demonstrated before (see the works of Charlamov) that this may be possible for some of the TIA architectures such as those based on resistive feedback, where the very same feedback resistance R_{F} defines both the gain and the noise level. However, for the case of a non-specific TIA architecture, this simple approach may render itself problematic due to interplay of several amplifier parameters. Still, from the analysis above we can approximately estimate the noise levels achievable for the target 1 GHz bandwidth using the best reported designs in 0.18 μm CMOS. For example, in series of works of Shahdoost it was demonstrated that around 3 pA/$\sqrt{\mathrm{Hz}}$ noise current density may be achieved using capacitive feedback TIA. Here we can set a more pessimistic upper bound of 5 pA/$\sqrt{\mathrm{Hz}}$ over the complete bandwidth, because this noise level shall be possible for a carefully designed circuit. Moreover, with this extra margin we can also accommodate the noise of the APD which was ignored in the analysis of the TIA architectures as presented above. Assuming for simplicity constant current noise over the bandwidth, the noise equivalent power can be computed:

$$P_{\mathrm{NEP}} = i_{\mathrm{tot}} R_{\mathrm{T}}, \tag{1.58}$$

where i_{tot} is computed as the square-root from the sum of all noise sources multiplied by the bandwidth:

$$i_{\mathrm{tot}} = \sqrt{\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} BW}. \tag{1.59}$$

The value of S in the numerator of DR is obtained for the case of APD as follows:

$$S = \frac{Bs \cdot T_0 \cdot P_0 \cdot \eta \cdot M \cdot R_{\mathrm{T}}}{4}. \tag{1.60}$$

In the expression above M is the APD multiplication factor, η is the PDs quantum efficiency and R_{T} is the TIA gain (for example, approximated as R_{F} for classical resistive feedback TIA) and the rest of the parameters being the same as in the calculation of ADZ. The expressions above provide the methodology for spec-

ifying the required gain of the TIA if noise equivalent power is found or can be assumed. For a typical APD it can be shown that the required 50 dB DR can be achieved with R_{T} of approximately 500 kΩ and is better than state-of-the-art OTDR instruments reported at the market (e.g. see (VeEX, 2022)). Note here that the maximum achievable DR is obtained at the price of increased ADZ. Differently from the resistive feedback TIA discussed by Charlamov, the gain and the noise of the amplifier may be caused by different components of the circuit and one cannot generalize for a simple dependency such as square-root dependency on R_{F}. This assumption only works for particular TIA architecture which, one shall admit, was for a longer time the de facto standard when designing TIAs. Similar procedure can be applied if different combinations of the gain and bandwidth are necessary. Note that in order to get alternative ADZ and DR combinations we also shall not follow a simple process of the filtering as it had been demonstrated that better noise scaling is obtained with programmable-gain configurations (Charlamov et al., 2012). Although the original work on OTDR-specific TIA (Charlamov & Navickas, 2015) reported a variable gain SFB TIA, a practical implementation with new envisioned topology may be non-trivial if the rest of the constraints needs to be fulfilled with a single global TIA structure. Furthermore, depending on the topology finally chosen for TIA, it can be difficult to implement variable gain when changing only one circuit parameter (i.e. such as implemented with feedback resistor in (Charlamov & Navickas, 2015) or (Yeom et al., 2019)) and advanced design methodologies may be needed including simultaneous adjustment of several elements. For simplicity we do not set any specific requirements for the phase linearity and group delay variations for the TIA while those can be hardly mapped to the most important OTDR parameters such as ADZ and DR.

The developed set of requirements is shown in Table 1.3. Out of these preliminary requirements, one should point the requirement of relatively low noise requirement (below 5 pA/$\sqrt{\mathrm{Hz}}$) for the given bandwidth. This limits our design to that which is believed to achieve such low noise levels - capacitive feedback TIA and eliminates most of the standard high-speed architectures and designs typically used for OTDR application - i.e. classical resistive shunt-feedback TIA with or without the feedback capacitor C_{F} (Charlamov & Navickas, 2015; Yeom et al., 2019). We also try to avoid widely adopted techniques of inductive broad-banding or those shall be applied with greater care. As the work addresses the design of a single-channel TIA, no special consideration for crosstalk performance is required, while particular treatment is expected to ensure the specification conformance for a broader range of transimpedance gains. Finally, no constraints are given in terms of the chip area, although, naturally, one should seek area minimization when targeting commercial low-cost applications. Note that the design of TIA as an integrated circuit leads to increased flexibility in circuit tuning and noise optimization via the device geometry adjustment, when compared to the design with discrete compo-

nents. Here special design optimization techniques can be used to find optimal values for the geometry of separate elements. This becomes an important feature that is simply not possible when designing the TIA from discrete components.

Table 1.3. Preliminary CMOS TIA specification for OTDR application

Parameter	Target Value
-3 dB bandwidth	0.1-1 GHz @ min. gain of 5 kΩ preferred gain. 10 kΩ
Noise power spectral density	< 5 pA/$\sqrt{\text{Hz}}$ @ 500 MHz
Gain	Variable: 10, 25, 100, 200, 500 kΩ
Input capacitance	0.2 pF
Photodetector capacitance	0.5 pF
Quiescent power	< 50 mW
Technology	CMOS / BiCMOS
Operating temperature range	Industrial (-40…+85°C)
Power supply voltage	1.8 V - 2.5 V

The TIA shall be designed to operate with the C_{D} as large as 500 fF and input capacitance (ESD, pad, etc.) of additionally 200 fF. The need to support such large capacitances arises due to higher performance PDs being external to the chip with correspondingly large bond-pad capacitances. A lower input capacitance would permit a higher input impedance and allow smaller devices to be used in TIA resulting in substantial power savings, while retaining the same bandwidth and improved sensitivity or increased bandwidth with equivalent sensitivity. The quiescent power requirements are due to the maximum power allocated for optical receiver front-end in envisioned handheld instrument. Note here a complete industrial temperature range requirement which is broader than that of typical higher performance instruments (LUCIOL, 2021, 2022).

As CMOS technologies with a feature size of 0.35 µm, 0.25 µm and 0.18 µm become available for small volume production with f_{T} close to 13.5 GHz, 18.6 GHz and 49 GHz correspondingly and bearing in mind that transistor can be operated at $f_{\text{T}}/10$, these submicron CMOS technologies can be easily used for IC production with upper frequencies of 1.35, 1.86 and 4.9 GHz respectively (Safar & Zaki, 2013). Thus, the choice of 0.18 µm CMOS provides a sufficient margin for the intended application according to the bandwidth requirements presented above. Moreover, the work of (Shahdoost et al., 2016) had demonstrated that parameters close to our target specifications can be reached for capacitive feedback architecture already using 0.18 µm CMOS and hence this technology seems to be a good compromise between achievable performance and price. The closest in performance and available for small series prototype development BiCMOS is the

0.25 μm process from IHP Microelectronics. Note that from BiCMOS we choose the CMOS part for our design because of several reasons. First, our target is to design and implement TIA in CMOS due to its price and integration advantages over the plain bipolar technology. This is extremely important if we want to have the flexibility to change the foundry service later or integrate the TIA into a complete OTDR ASIC. Moreover, our selected capacitive feedback architecture was shown to perform the best when implemented in CMOS and it goes beyond this dissertation to verify if this architecture in general scales up for bipolar design. Clearly, the power supply voltage is strongly related to the technology to be used and the requirement to have supply voltage in the range 1.8 V-2.5 V fits quite well typical voltages of 0.18 μm CMOS and 0.25 μm BiCMOS.

Based on the results above we can compute the required FOM for our CMOS TIA. Taking the upper bound for the power consumption as 50 mW and target noise as 5 pA/$\sqrt{\text{Hz}}$ we obtain the specification requirements in terms of FOM to be equal to 28.0 for the most pessimistic gain configuration with simultaneous gain of R_{T} of 10 kΩ and bandwidth of 1 GHz. Although, when viewed from a FOM perspective, the specification seems to be satisfied by numerous designs, we will still aim for the best design margin possible to ensure that a realistic circuit will still meet the requirements. Clearly, the capacitive feedback design elaborated in the series of works of Shahdoost is the best candidate to serve as the basis for implementation as the reported FOM equal to 114 (correspondingly 45 for 0.18 μm design) is above our requirement and is the largest for designs reported for 1–2 GHz.

1.5. First Chapter Conclusions and Formulation of the Thesis Objectives

The analysis presented in Chapter 1 can be summarized with the following concluding statements:

1. The tremendous growth of Internet traffic in recent years has led to the rapid development of broadband optical communication systems. Although possessing numerous advantages, the communication systems based on optical fibers may still suffer from mechanical, environmental and natural deterioration. This, in turn, increased the demand for equipment to monitor, maintain and repair fiber-optic data network. OTDR is one of the typical and most important instruments employed for fault detection and characterization. The most important parameters of such instrument (dynamic range, dead zone) are typically limited by the performance of the front-end TIA. The front-end TIAs of the modern OTDR instruments are typically built from the discrete components with very limited band-

width, suboptimal characteristics and significant parasitics. Therefore, it is important to develop new TIA architectures and corresponding ICs to be used in next-generation high-performance OTDR systems.

2. In order to assess qualitatively different TIA architectures we suggest to employ a new figure-of-merit (FOM) which combines the following main TIA parameters: bandwidth, transimpedance gain, total input capacitance, power consumption, and input-referred noise current spectral density.
3. Based on the suggested FOM, an analysis of different TIA architectures was performed which allowed to identify six main TIA families: classical resistive feedback TIA (optionally combined with feedback capacitance), inverter-based feedback TIA, common-gate TIA, regulated cascode TIA, TIA with inductive peaking and capacitive feedback TIA. The latter architecture reported the best FOM for applications with bandwidth of several GHz, reaching FOM values of 114.
4. Based on the analysis of scientific publications and reported commercial products, a set of the main parameters for the front-end TIA to be achieved has been developed which would enable the development of next-generation OTDR instruments.

The above conclusions lead to the following tasks that form the dissertation problem:

1. Develop a novel capacitive feedback programmable-gain TIA architecture with associated gain and noise mathematical models which will enable development of broadband ($\geq$1 GHz) low-noise ($\leq$5.0 pA/$\sqrt{\text{Hz}}$) TIAs.
2. Design and investigate integrated circuits implementing the proposed TIA architecture using modern 0.18 μm CMOS and 0.25 μm BiCMOS technologies.

2

Capacitive Feedback TIA Model Development and Investigation

In this chapter, the theoretical models of the selected TIA architecture are developed and discussed. The analysis starts with the discussion of the generic capacitive feedback approach. First, an initial implementation is proposed with a pure resistive biasing and a more accurate mathematical model for the description of the circuit behavior in low-frequency range. Later, an area-efficient PMOS-based implementation for the biasing is suggested along with additional modifications to the reference architecture. A programmable-gain approach is developed with simultaneous adjustment of one of the feedback capacitors and the resistance in the biasing circuit. Finally, an improved programmable-gain configuration is proposed with cascode implementation of the current source in the source follower and gain adjustment using only a single parameter. A corresponding noise model for a generic capacitive feedback approach is developed and discussed.

The research results, presented in this chapter, have been already partially demonstrated and discussed at international "MTTW" (Romanova & Barzdenas, 2019b), "MIXDES" (Romanova & Barzdenas, 2020c) and "eStream" (Romanova & Barzdenas, 2020b) scientific conferences as well as published in (Romanova & Barzdenas, 2020a) paper.

2.1. Capacitive Feedback TIA

Even though a differential configuration offers a number of advantages, especially in CMOS technology, a single-ended design is demonstrated in this work. The common-mode rejection property which is inherent in differential circuit makes it far more manageable to integrate TIA with noisy digital circuitry or with other TIA in an array with a minimal cross-talk. However, this argument is of less relevancy for the presented stand-alone single-channel TIA as it is not integrated into a complete circuit such as a dedicated OTDR ASIC (Tao & Berroth, 2003). The second argument for the differential design is due to the small transconductance of the typical MOS transistor which often results in achieving the required high open-loop gain by cascading several stages of relatively low gain and high bandwidth. However, cascading e.g. three stages in single-ended design may result in excessive phase shift and poor stability due to the presence of three secondary poles. Here a differential architecture may suffice with just two gain stages resulting in a more stable amplifier when compared to a multi-stage single-ended design. Nevertheless, this argument may be also of lesser importance as long as we are able to achieve the required gain and bandwidth without additional post-amplifier while a simpler structure of single-ended TIA will ensure reduced noise and smaller power consumption compared to the differential approach[1]. Still, single-ended amplifiers may have a tendency to common-mode oscillations especially when the impedance gain is very high as have been pointed out in (Tao & Berroth, 2003).

Since the transistor threshold voltage generally does not decrease as fast as feature size and the power supply voltage, an implementation of a higher performance TIA may also face challenges as many cascaded or folded designs may become not possible with reduced voltage supply. As the reduction in headroom voltage reduces the ability to cascode devices, low voltage and high-gain TIA configurations are often built with outward expanding, where two or even three cascaded amplification stages are used. However, these multi-stage cascaded designs may require to take extra measures to ensure the amplifier's stability and, depending on the topology, can be challenging or complex to stabilize. Furthermore, if one goes for cascaded design, the stabilization scheme may also require compensation capacitors and/or nulling resistors which can significantly increase the silicon footprint and decrease the amplifier's bandwidth. Bearing the stability issue in mind we will try to address the headroom voltage issue while staying with non-cascaded implementation.

[1]The reasons for the differential approach are exactly relevant when designing classical optical receivers and therefore differential designs are typically implemented for optical data communication, where the front-end shall support multiple channels and is integrated with the main amplifier, data decision, clock recovery, demultiplexing circuits, etc.

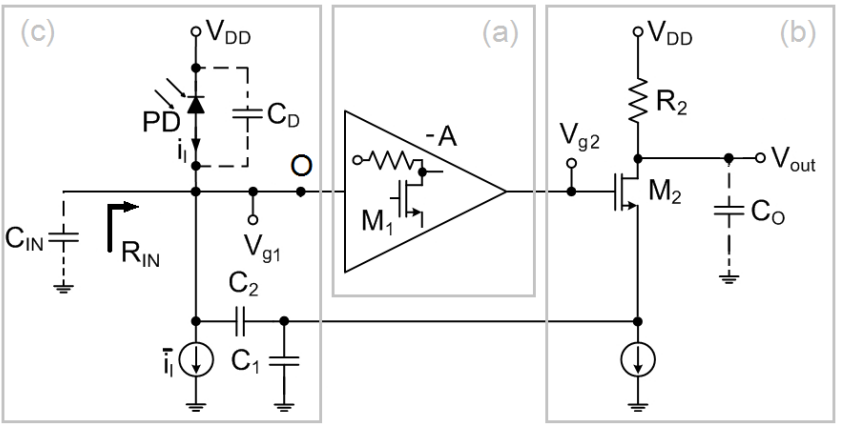

Fig. 2.1. Capacitive feedback TIA with denoted major blocks: (a) forward gain block; (b) source follower block; (c) feedback block

As we have seen in the previous chapter, the classical resistive-feedback TIA has an inherent problem with the noise performance of the feedback resistor R_{F} as it is directly added to the input-referred noise current and therefore drastically degrades the noise figure of the design. The classical resistive feedback design clearly trade-offs among the key TIA parameters such as noise, gain and bandwidth, where large values of R_{F} are needed to lowering noise and increasing the gain. It is not only that large value of R_{F} may be limited by maximum realizable on-chip resistance, but also that the value of R_{F} directly lowers down the bandwidth of the amplifier. Thus, it may be inevitable to introduce some structural changes to the reference TIA design to obtain an additional degree of freedom in expressions for noise and bandwidth. On the other hand, the feedback approach itself has important structural benefits as it ensures almost constant transimpedance gain in the bandwidth of interest while decreasing the sensitivity to process and temperature variations. Therefore, it may be beneficial to keep the general feedback structure of the amplifier, while substituting the noisy feedback resistor with a less noisy or completely noise-free element. An intuitive candidate for such a noise-free element is a capacitor. However, a direct replacement of R_{F} with a capacitor will result in a phase shift which requires a subsequent stage for phase correction. In this work, we follow an alternative approach shown previously in Fig. 1.16 and extended in Fig. 2.1 with separate blocks corresponding to the forward gain (block (a)), source follower (block (b)) and the feedback circuit (block (c)).

Based on our discussion in Chapter 1, transimpedance gain (mid-frequency approximation) for this generic architecture can be approximated as:

$$R_{\mathrm{T}} = \left(1 + \frac{C_1}{C_2}\right) R_2. \tag{2.1}$$

The simplified expression from above assumes an infinite forward gain A with the overall gain determined by the feedback circuit only formed by the feedback capacitors C_1 and C_2. It also does not consider some signal short by the bias resistance at the input and, therefore, suggests a somehow different gain when compared to the one obtained in the realistic circuit under typical CMOS constraints such as available voltage headroom. Although the expression can be used for a very rough analysis of the design, it is not extremely helpful if one wants to predict accurately the performance of a real circuit and, therefore, more accurate models are needed. Below we provide a more detailed model for the aforementioned feedback concept including modeling of the additional terms such as those due to biasing circuits, etc.

2.2. Fixed-Gain Configuration With Resistive Biasing

In order to develop a practical TIA circuit for OTDR application, one shall start with a detailed model of the corresponding fixed-gain configuration. In order to obtain a more comprehensive understanding of the frequency response, the complete transimpedance function of the amplifier shall be derived first. Before we go to the explicit modeling of the circuit, let us consider the simplified structure as shown in Fig. 2.1. This minor extension of the generic solution shown in Chapter 1 employs the voltage amplifier, the second stage with M_2 and a capacitive feedback network formed by two capacitors C_1 and C_2. If one ignores the source follower formed by M_2, then a relatively simple circuit formed by the forward gain (open-loop gain) G_1 and the feedback component F_1 can be assumed. It is important that the feedback gain is formed not only by the obvious capacitors C_1 and C_2, but also includes the effect due to total input capacitance C_{T}. Under these constraints the overall gain becomes the one of the classical feedback structure:

$$G_{\Sigma} = \frac{G_1}{1 + G_1 F_1}. \tag{2.2}$$

What remains unmodelled here is the impact of the source follower formed by M_2. There are two effects of the source-follower on the transfer function above. First, it clearly affects the open-loop gain G_1 via an additional factor G_{SF}. Moreover, due to the structure of the source follower with M_2, there is also a general feed-out gain G_{out} which resides outside the feedback loop. If we assume the design with the source follower, the expression above needs to be modified resulting in:

$$G_{\Sigma} = \frac{G_1 G_{\mathrm{SF}}}{1 + G_1 G_{\mathrm{SF}} F_1} G_{\mathrm{out}}. \tag{2.3}$$

A circuit-level design of the proposed amplifier is shown in Fig. 2.2. This detailed view allows us to split further the gain component G_{SF} of the source follower into two parts. One gain component G_2 is the high-pass filter formed by the C_{C} and the biasing circuit for M_2, while the second gain component G_3 is solely due to the source follower itself. The overall voltage gain transfer function G_Σ of the circuit can be derived from the combined forward gain $G_1G_2G_3$ (input stage, high-pass circuit and source follower), the feedback gain component F_1 and the output feed-out gain G_{out} as:

$$G_\Sigma = \frac{V_{\mathrm{out1}}}{V_{\mathrm{in}}} = \frac{G_1G_2G_3}{1 + G_1G_2G_3F_1}G_{\mathrm{out}}. \tag{2.4}$$

Note that one can also ignore the component G_2 due to the C_{C} and the biasing for M_2 and get a simplified closed-loop expression gain:

$$G_{\Sigma'} = \frac{V_{\mathrm{out1}}}{V_{\mathrm{in}}} = \frac{G_1G_3}{1 + G_1G_3F_1}G_{\mathrm{out}}. \tag{2.5}$$

Whether to use a more accurate or simplified model without G_2 depends on our interest in the model covering the high-pass behavior of the circuit, as we will see later.

While preserving the general structure of the capacitive feedback, one still has some flexibility in selecting the structure of the core operational amplifier. We want to minimize the noise integrated across a moderate bandwidth of 1 GHz, therefore we select a single input stage to minimize the number of the active elements contributing the noise. Here we followed a classical approach of using a modification of the single-stage common-source amplifier as shown in Fig. 2.2, although alternative solutions for core voltage amplifier can also be used (Hu et al., 2010a,b). The transistor's output resistance decreases with the scaling down and, as a result, the intrinsic voltage gain of the transistor becomes smaller opting for using multi-stage configuration. However, the usage of multistage amplifiers increases the overall power consumption and may affect the amplifier's stability. Obviously, one shall ensure that sufficient gain is achieved with the provided CS configuration. For low-noise applications, the CS stage can be considered as a viable option when compared to alternative more complex implementations.

Some words are probably needed on whether the source follower shall be used at all. First of all, the source follower isolates R_1 from the loading effect of the capacitive feedback (formed by C_1 and C_2) as well as input capacitance of the subsequent stage, because this loading effect may result in lowering the bandwidth and decreasing stability by introducing yet another dominant pole across R_1. The additional penalty comes from the need for a biasing circuit for M_2, which would require resistors whose noise would generally add to the noise of the final system.

On the other hand, as the technology scales down, the constraints may limit the realization of the source follower stage in the proposed TIA design. In principle, one could also have tried to implement the capacitive feedback directly from M_1 (as it is sometimes done for classical SFB TIA, see e.g. (Keshri, 2010)) while avoiding source follower stage in the feedback. Similarly although the input noise is expected to be somehow lower for the configurations without source follower, in the version with source-follower one may achieve the required bandwidth easier due to its lower input resistance and, because of the isolation behavior of M_2, it may be easier to tune the complete design. Due to latter reasons we decided to stay with the design using source-follower. As we will see, the biasing circuit for M_2 will indeed impose some challenges due to voltage headroom for our 1.8 V power supply and special circuit-level measures shall be taken for an area-efficient implementation. Still, if one thinks on scaling down the design for even lower power supply voltages, it may leave the designer no other option as to discard the source-follower whatsoever.

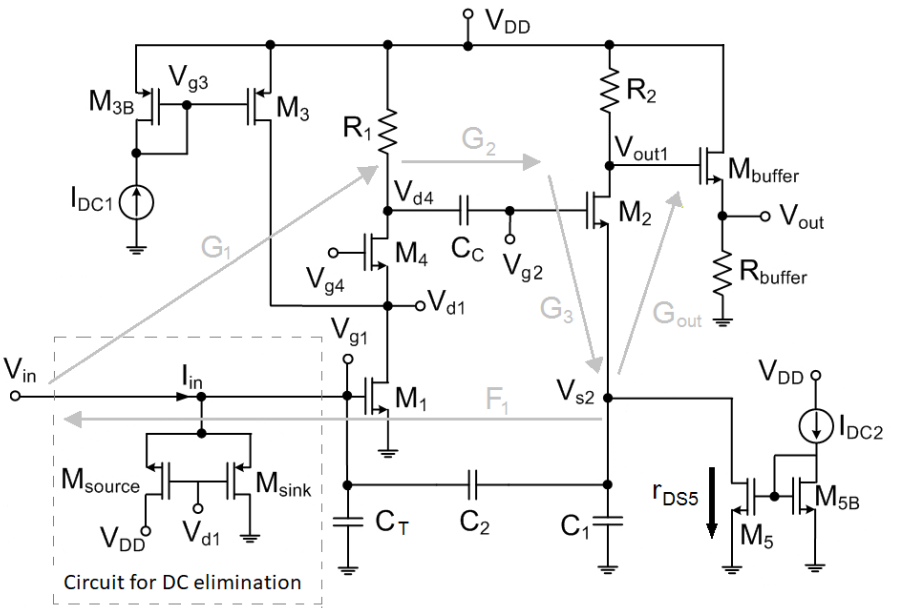

Fig. 2.2. An implementation of a fixed-gain capacitive feedback TIA. For simplicity, the PDs capacitance and the input capacitance are replaced with a single equivalent capacitance C_{T}

In both expressions above one defines the gain for the input CS stage with M_1 and R_1 as:

$$G_1 = \frac{V_{\mathrm{d4}}}{V_{\mathrm{in}}} = g_{\mathrm{m},1} R_1. \tag{2.6}$$

The expression above ignores the impact of the cascode transistor M_4. Often the CS stage also employs an inductive peaking to increase the bandwidth of the open-loop amplifier. We do not use this option, because we target inductor-less design and the 0.18 µm CMOS has sufficient f_{T} for 1 GHz applications. The second gain component considers the influence of the biasing resistor of the second stage $R_{\mathrm{bias,2}}$ and capacitive isolation C_{C} and can be written with $s = j\omega$ as:

$$G_2 = \frac{V_{\mathrm{g2}}}{V_{\mathrm{d4}}} = \frac{sR_{\mathrm{bias,2}}C_{\mathrm{C}}}{1 + sR_{\mathrm{bias,2}}C_{\mathrm{C}}}, \tag{2.7}$$

with the resistive biasing circuits shown in Fig. 2.3 (a) for M_1 and Fig. 2.3 (b) for M_2. The term controls the high-pass behavior, where an introduction of the capacitor in the connecting path between M_1 and M_2 shall also help in mitigating the voltage headroom constraints on R_1 and hence its value can be also increased to minimize the thermal noise component. As discussed before, this component is responsible for the high-pass behavior. If we skip this component as suggested in definition of $G_{\Sigma'}$, the model will demonstrate no attenuation down to DC. Since G_2 as defined above is a classical first-order high-pass filter with time constant:

$$\tau_{\mathrm{G_2}} = R_{\mathrm{bias,2}}C_{\mathrm{C}}, \tag{2.8}$$

and corresponding cutoff frequency:

$$f_{\mathrm{c,G_2}} = \frac{1}{2\pi\tau_{G_2}} = \frac{1}{2\pi R_{\mathrm{bias,2}}C_{\mathrm{C}}}. \tag{2.9}$$

Since the biasing circuit for M_2 requires resistors, their thermal noise contribution will add to the noise of the system. As for practical implementations, C_{C} must be implemented with a MIM capacitor since it is in the signal path. The last gain component is caused by the source-follower M_2 and can be written:

$$\begin{aligned} G_3 &= \frac{V_{\mathrm{s2}}}{V_{\mathrm{g2}}} = \frac{g_{\mathrm{m,2}}r_{\mathrm{DS5}}}{1 + sr_{\mathrm{DS5}}\left(C_1 + C_2\right) + g_{\mathrm{m,2}}r_{\mathrm{DS5}}} \\ &= \frac{g_{\mathrm{m,2}}r_{\mathrm{DS5}}}{1 + g_{\mathrm{m,2}}r_{\mathrm{DS5}}} \cdot \frac{1}{1 + s\frac{r_{\mathrm{DS5}}(C_1+C_2)}{1+g_{\mathrm{m,2}}r_{\mathrm{DS5}}}} \approx \frac{1}{1 + s\frac{(C_1+C_2)}{g_{\mathrm{m,2}}}}, \end{aligned} \tag{2.10}$$

with simplifications possible due to $g_{\mathrm{m,2}}r_{\mathrm{DS5}} \gg 1$. As typically $C_1 \gg C_2$, one

may also use a simpler formulation:

$$\begin{aligned} G_3 &= \frac{V_{\rm s2}}{V_{\rm g2}} \approx \frac{g_{\rm m,2} r_{\rm DS5}}{1 + s r_{\rm DS5} C_1 + g_{\rm m,2} r_{\rm DS5}} \\ &= \frac{g_{\rm m,2} r_{\rm DS5}}{1 + g_{\rm m,2} r_{\rm DS5}} \frac{1}{1 + s \frac{r_{\rm DS5} C_1}{1 + g_{\rm m,2} r_{\rm DS5}}} \approx \frac{1}{1 + s \frac{C_1}{g_{\rm m,2}}}. \end{aligned} \tag{2.11}$$

As we mentioned before, the capacitive feedback is implemented from the source follower to isolate R_1 from the leading effect of both the feedback circuit and the input capacitance of the subsequent stage. Thus, the parameters of the capacitive feedback circuit can be adjusted without an explicit impact on headroom constraints[2]. The voltage headroom constraints may make the realization of the source follower stage in the TIA design a challenging task and special efforts may be necessary to implement the approach under given power supply constraints.

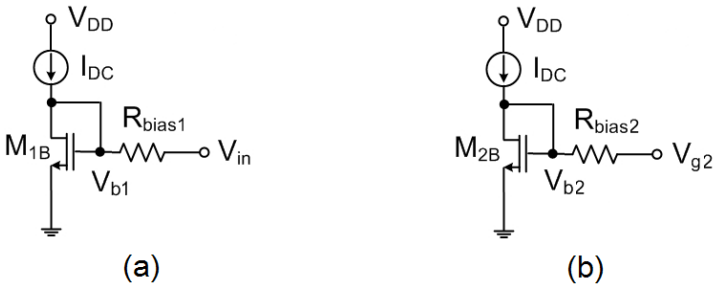

Fig. 2.3. Resistive biasing circuits: (a) biasing circuit for M_1; (b) biasing circuit for M_2

The feedback component becomes approximately:

$$\begin{aligned} F_1 &= \frac{V_{\rm in}}{V_{\rm s2}} = \frac{R_{\rm bias,1}}{R_{\rm bias,1} + \frac{1}{sC_2} + R_{\rm bias,1} \frac{C_{\rm T}}{C_2}} \\ &= \frac{s R_{\rm bias,1} C_2}{1 + s R_{\rm bias,1} C_2 + s R_{\rm bias,1} C_{\rm T}} = \frac{s R_{\rm bias,1} C_2}{1 + s R_{\rm bias,1} \left(C_{\rm T} + C_2\right)}, \end{aligned} \tag{2.12}$$

and includes the influence of the total input capacitance $C_{\rm T} = C_D + C_{\rm IN}$ with an additional path neglected due to $C_2 \ll C_1$. Finally, the last factor can be shown to be:

$$G_{\rm out} = \frac{V_{\rm out1}}{V_{\rm s2}} = R_2 \frac{1}{Z_{\rm s2}} = R_2 \frac{1 + s r_{\rm DS5} \left(C_1 + C_2\right)}{r_{\rm DS5}}, \tag{2.13}$$

[2]The design idea is also often used in SFB TIA, see, for example, (Keshri, 2010).

where the impedance:

$$Z_{\mathrm{s2}} = \frac{r_{\mathrm{DS5}}}{1 + s r_{\mathrm{DS5}} \left(C_1 + C_2\right)}. \tag{2.14}$$

Here the expression includes a zero formed by $C_1 + C_2$ and r_{DS5} and obvious approximation is possible as $C_1 \gg C_2$. The pole due to the load capacitance would appear also outside the loop and as long as R_2 is less than the drain-source resistance of M_1, the stability of the amplifier is not determined by the value of R_2. This property allows for a different set of trade-offs between gain, noise and bandwidth when compared to the classical resistive feedback approach. As a possible optimization one can also implement the R_2 as an active PMOS load in order to maximize the gain of the TIA.

For the transimpedance gain Z_{T} the current-voltage transformation at input impedance shall be considered:

$$\begin{aligned} Z_{\mathrm{T}} &= \frac{V_{\mathrm{out1}}}{V_{\mathrm{in}}} \cdot \frac{V_{\mathrm{in}}}{I_{\mathrm{in}}} = G_{\Sigma} Z_{\mathrm{in}} = G_{\Sigma} \frac{X_{\mathrm{C}} \cdot R_{\mathrm{bias,1}}}{X_{\mathrm{C}} + R_{\mathrm{bias,1}}} \\ &= G_{\Sigma} \frac{R_{\mathrm{bias,1}}}{1 + s R_{\mathrm{bias,1}} \left(C_{\mathrm{T}} + \frac{C_1 C_2}{C_1 + C_2}\right)}. \end{aligned} \tag{2.15}$$

For the total input impedance we consider C_{T} connected in parallel with series connection of C_1 and C_2. The latter component is approximately equal to C_2. Furthermore, $C_{\mathrm{T}} \gg C_2$ one can simplify the expression and get:

$$Z_{\mathrm{T}} = G_{\Sigma} Z_{\mathrm{in}} \approx G_{\Sigma} \frac{R_{\mathrm{bias,1}}}{1 + s R_{\mathrm{bias,1}} C_{\mathrm{T}}}. \tag{2.16}$$

Important is that the expression above does not assume the bias circuit being perfect. However, if this assumption is valid, then using the L'Hopital's rule:

$$\lim_{x \to a} \frac{f(x)}{g(x)} = \lim_{x \to a} \frac{f'(x)}{g'(x)}, \tag{2.17}$$

one can get:

$$\lim_{R_{\mathrm{bias,1}} \to \infty} Z_{\mathrm{in}} = \frac{1}{1 + s \left(C_{\mathrm{T}} + \frac{C_1 C_2}{C_1 + C_2}\right)} \approx \frac{1}{1 + s C_{\mathrm{T}}}. \tag{2.18}$$

In the expression above G_{Σ} is not the voltage, but the dimensionless voltage gain, which makes the overall expression consistent in terms of units.

The expressions above hold only when the operating point of the input stage transistor M_1 is established. The operating point can be controlled by the current source in parallel with R_1. As we are targeting a programmable-gain configuration, the current source formed by M_3 shall consistently fit and be aligned with all the required configurations developed below. The presented design is believed to have several major advantages over other well-established designs. First of all, the major part of the gain definition network is still mainly formed by C_1 and C_2 and therefore should introduce much less noise compared to resistive feedback. Furthermore, the total noise current contributed by the first stage shall be significantly lower compared to that of SFB TIA for the given bandwidth. Finally, the capacitance as seen at the input node shall not degrade the stability of the design and shall only lower the DC loop gain. With proper design, the noise contribution of M_2 may be also made negligible. The architecture also resembles the generic behavior of topologies such as CG where the noise of the current mirror directly adds to the noise current of R_2. At the same time, when compared to simple feed-forward designs, the noise current of R_2 is divided by Z_{T} (or approximation $(1 + C_1/C_2)$ for Z_{T}). Note that the proposed design allows us to achieve the bandwidth requirements without any inductive enhancement.

The classical CS structure of the voltage amplifier can be improved using the cascode implementation with an additional NMOS (M_4) stacked on the top of M_1. Because of its high output resistance, the voltage gain of the cascode structure is higher than that of the regular one. The bandwidth of this cascode TIA may be also improved due to reduction of the Miller capacitance of C_{gd} in M_1 which is a part of the input capacitance and which due to high gain requirement may have a significant impact on the amplifier performance. This degradation is particularly significant in CMOS circuits, where the gate-drain capacitance can be as high as one-third of the gate-source capacitance (Mohan et al., 2000). Technically the Miller capacitance is canceled because the input impedance of CG-connected M_4 represents the load of transistor M_1, while the drain of M_1 will see low impedance. The M_4 is biased to the lowest value that keeps the M_1 in saturation region during the operation (i.e., in our case 1.4 V via V_{g4}). Thus, the design shall contribute to the overall noise efficiency of the amplifier.

The quality of the feedback mainly depends on the gain of the internal operational amplifier. However, a naive approach to increase the value of R_1 is likely to fail due to issues related to the voltage headroom problems for the envisioned 1.8 V power supply. A solution to the problem is to implement a so-called *gain boosting*, where an alternative path to the drain current is provided with a PMOS transistor M_3 added to operate in parallel with R_1 and to handle the current fed to M_1. The noise contribution of M_3 is minimized by biasing it with a large overdrive voltage generated by the shown current mirror formed by M_{3B}. As a result, one may increase the value of R_1 while keeping the current density in M_1 suffi-

ciently high. In both paths, one shall also try to decrease the corresponding noise currents. While for R_1 this may be achieved by simply increasing R_1, the noise current minimization for M_3 may be achieved by proper biasing. A dedicated bias circuit is designed to minimize the noise contribution of M_3. The new transistor may introduce high drain current noise of its own, which may negate the effect of increasing R_1 to reduce thermal noise. Hence, proper design considerations with respect to noise analysis shall be taken into account. With all this in mind, the circuit is configured with 80% of the current fed via M_3 and the rest passing through the original R_1. The approach not only reduces the noise contribution of the load, but also a relatively high gain of this simple core amplifier may be reached.

Special handling of the DC dark current is also necessary for the TIA of the given topology. If not addressed properly, it may lead to saturation issues and instability. Here we follow the general strategy with a pair of transistors placed at the gate of M_1. The NMOS device operates as a current source while the PMOS operates as a current sink (see DC eliminator block in Fig. 2.2). Both added transistors are off at the absence of input DC current. In the excess of DC current sourcing to the gate of M_1, the diode-connected transistor will sink the extra current to the ground while limiting the maximum voltage at the gate of M_1. In case of extra DC current-sinking from the input node, the M_{source} has to turn on and will provide an extra current. This transistor is off in the absence of the extra sinking current and will turn on only if simultaneously the voltage at the gate of M_1 drops and the voltage at the drain increases. Both transistors are optimally designed with minimum widths to reduce the input noise current of the circuit. The activation time period of this pair is very short which, on average, shall result in a negligible noise contribution to the overall input noise current of the circuit. The transistors shall be also designed with minimum possible widths to minimize their thermal current noise.

In order to match the output of the TIA to 50 Ω loads, as a requirement for most of the voltage-output amplifiers, a dedicated buffer stage is added to the output of the proposed topology. Here the transistor M_{buffer} is biased to have a transconductance $g_{\mathrm{m,buffer}}^{-1}$ = 50 Ω.

We shall note here that the developed transfer function G_Σ is different from the one suggested in series of works of Shahdoost. There, the author ended up with the following approximation for the current gain (Shahdoost et al., 2011):

$$\frac{I_{\mathrm{out}}}{I_{\mathrm{in}}} = \frac{\frac{A(C_1+C_2)+C_2}{C_{\mathrm{T}}+C_2+AC_2}}{1+\frac{s(C_1C_{\mathrm{T}}+C_1C_2+C_2C_{\mathrm{T}})}{g_{\mathrm{m},2}(C_{\mathrm{T}}+C_2+AC_2)}}, \tag{2.19}$$

which for the basic CS (see expression for G_1 above) voltage amplifier would result

in:

$$Z_{\mathrm{T,Sh}} = \frac{V_{\mathrm{out}}}{I_{\mathrm{in}}} = \frac{R_2 \frac{g_{\mathrm{m},1} R_1 (C_1 + C_2) + C_2}{C_{\mathrm{T}} + C_2 + g_{\mathrm{m},1} R_1 C_2}}{1 + \frac{s(C_1 C_{\mathrm{T}} + C_1 C_2 + C_2 C_{\mathrm{T}})}{g_{\mathrm{m},2}(C_{\mathrm{T}} + C_2 + g_{\mathrm{m},1} R_1 C_2)}}. \tag{2.20}$$

The model above neither considers C_{C} nor includes the impact of the bias resistors $R_{\mathrm{bias},1}$ and $R_{\mathrm{bias},2}$ as well as current source r_{DS5}.

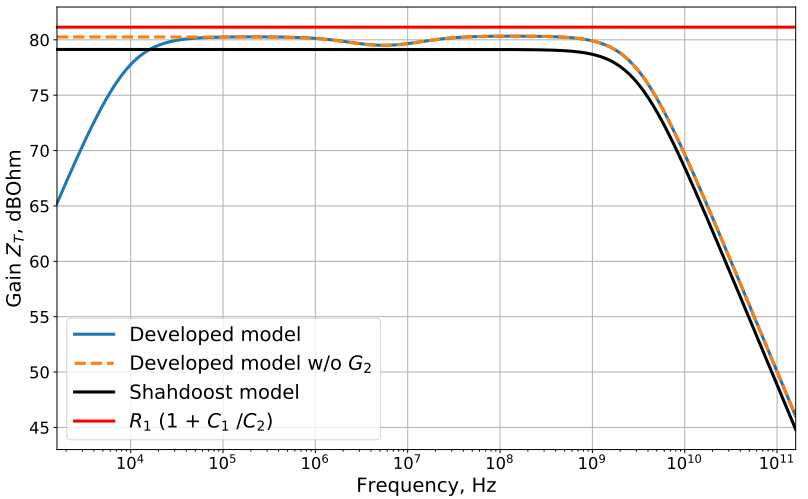

Fig. 2.4. Transimpedance gain of the developed and several simplified models for the exemplary TIA configuration of 10 kΩ

Let us have a look to the generic model behavior designed for an exemplary gain of R_{T} = 10 kΩ and without the buffer stage. Fig. 2.4 provides the gains of the corresponding three analytical models discussed previously along with a famous simplified constant-gain approximation and computed for the same set of circuit parameters. First, we see a difference in the gain plateau between our suggested model for the gain Z_{T} (complete model with G_2 component) and the model from the series of works of Shahdoost, because our model results in larger predicted gain when compared to the model of Shahdoost. Moreover, the latter model predicts constant gain down to the DC. As we discussed before, the high-pass behavior of our circuit is essentially defined by the filter formed by the decoupling capacitor C_{C} and $R_{\mathrm{bias},2}$ at the input of the source follower. Nevertheless, we cannot obtain the model of Shahdoost by simply removing the G_2 from the gain as we clearly see in Fig. 2.4. This is, however, not surprising as the model from Shahdoost makes further simplifying assumptions on current source I_{SS} as well as assumes perfect biasing at the input. Unfortunately, one clearly sees a two-region structure of the gain high- and low-frequency ranges controlled by different circuit parameters. It is

also important that the famous constant-gain approximation slightly overestimates the actual gain of the system for our configuration.

The same applies to the phase modeling as shown in Fig. 2.5. As expected, the model of Shahdoost is simply a first-order system, while our proposed model correctly takes into account the pass-band behavior of a realistic circuit with two phase transitions of 90 degrees visible. A small artefact in phase around 10^7 MHz corresponds exactly to the stitching point of two regions as we have seen in the gain plot. With some fine tuning one may be able if not eliminate, then to minimize this pitch, but for this example we explicitly avoided extensive tuning in order to demonstrate the underlying complex structure of the model. Note that exactly the G_2 component is responsible for the first phase shift, although the minor phase oscillations in the model without G_2 remain confirming that the model is not effectively identical to that of Shahdoost.

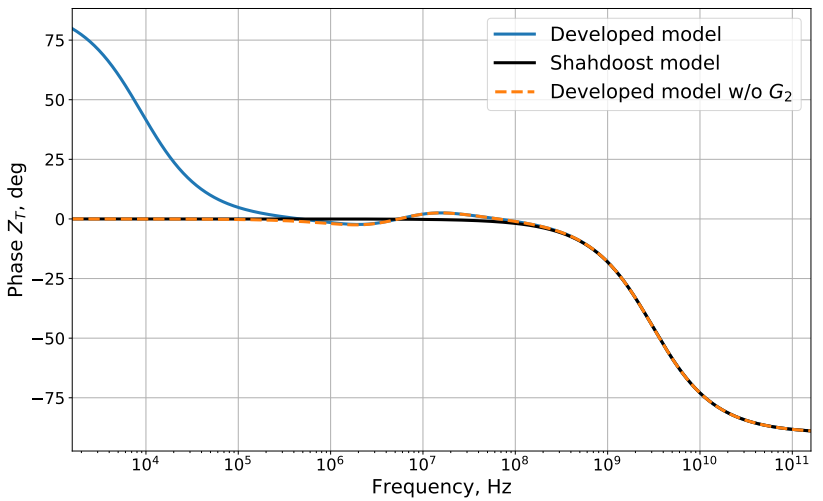

Fig. 2.5. Transimpedance phase of the developed and several simplified models for the exemplary TIA configuration of 10 kΩ

An important characteristic of any front-end amplifier is its input impedance Z_{in}. The input impedance and its real part are shown in Fig. 2.6 for the example configuration with R_{T} = 10 kΩ. As the PD can be modeled as a current source, we want to have a low input impedance. However, our circuit does not have as low input impedance as we would like to have. This means that the circuit is rather sensitive to the value of C_{T} when compared to some alternative implementations. As we have discussed in Chapter 1, dedicated TIA architectures have been developed (see CG and RGC TIA) to deal with this problem. Although our design does not have this useful decoupling feature, it was also not an explicit requirement.

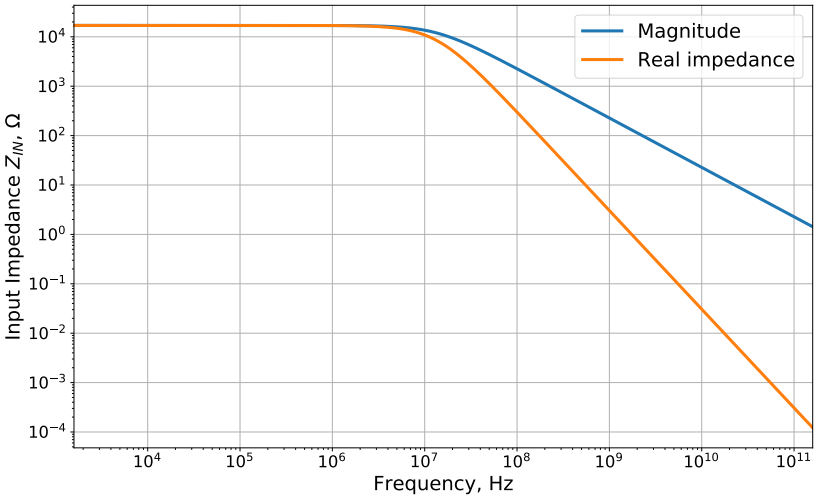

Fig. 2.6. Analytical results for input impedance of the developed model for the exemplary TIA configuration of 10 kΩ

Although the analytical expression for the transimpedance gain in all cases explicitly considers the design value for C_{T}, this value is only partially under the control of the designer and, in practice, the total input capacitance can be slightly different from the one assumed for the reference design. The sensitivity of the transimpedance gain with respect to the value of C_{T} can be seen in Fig. 2.7, where the circuit was designed assuming a reference value C_{T} of 0.7 pF. Although, in general, all frequency ranges are affected by varying C_{T}, the most prominent effect can be seen for mid- and high-frequency range. As expected, the actual value of C_{T} plays an important role in determining the bandwidth of the circuit with smaller C_{T} resulting in increased bandwidth. For comparison, the same sensitivity plot of the transimpedance gain is shown in Fig. 2.8 for the analytical model of Shahdoost. As we have seen before, the model of Shahdoost effectively results in TIA modeled as a first-order system (filter), where variation of the C_{T} results both in the gain change and obvious increase of the bandwidth for smaller C_{T}. Due to its complexity the results are not as simple for the proposed model Z_{T}, where not only bandwidth decreases with larger C_{T}, but the gain itself varies with the frequency. This effect is quite opposite in the competing model where both systematic increases in gain and bandwidth take place consistently and simultaneously. Interesting to note that the dependency on C_{T} affects the transfer function only after the region stitching point and the lower part of the gain plateau together with the lower corner frequency remain intact.

Still, both models consistently demonstrate a strong dependency of the bandwidth on the actual value of C_{T}. This observation is different from the results

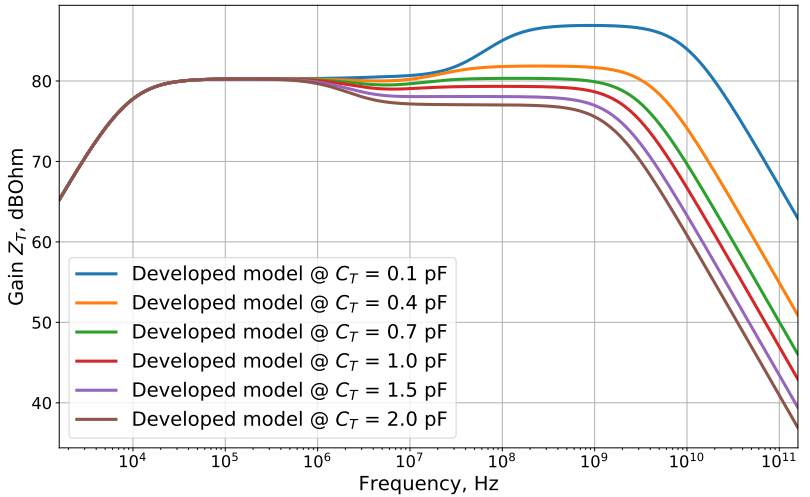

Fig. 2.7. Sensitivity of the transimpedance gain (proposed model) to the total input capacitance with design target $C_{\mathrm{T}} = 0.7$ pF and the exemplary TIA configuration of 10 kΩ

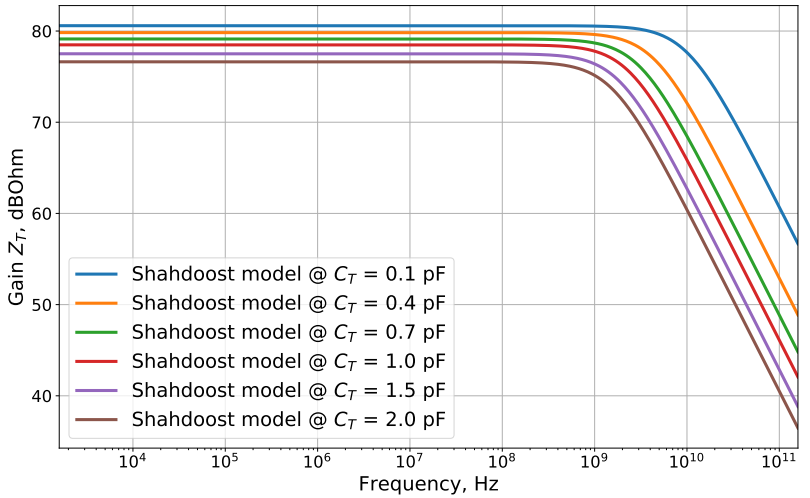

Fig. 2.8. Sensitivity of the transimpedance gain (Shahdoost model) to the total input capacitance with design target $C_{\mathrm{T}} = 0.7$ pF and the exemplary TIA configuration of 10 kΩ

reported in (Yiling Zhang et al., 2008), where the authors claimed the capacitive feedback TIA to perform better over conventional resistive feedback structure in terms of the bandwidth dependency on C_{T} value. Unfortunately, this feature of the capacitive feedback TIA cannot be directly deduced from our model or even

the model of Shahdoost, although the results reported by Zhang may also depend on a particular TIA parametrization and the dependency on C_{T} may be still better than that of classical SFB TIA. The obtained results can be also compared to those shown in (Yong-Hun Oh & Sang-Gug Lee, 2004), where the broadband cascode topology with inductance enhancement shunt peaking as the load was proposed. The authors in (Yong-Hun Oh & Sang-Gug Lee, 2004) also demonstrated the sensitivity of the developed circuit to the varying value of C_{T} and similarly to the results above, decreased value of C_{T} resulted in increased bandwidth. Nevertheless, based on these results we cannot claim that the capacitive feedback TIA is able to decouple the input capacitance from the bandwidth of the circuit. However, as we mentioned before, this nice-to-have feature was also not the target requirement for our design.

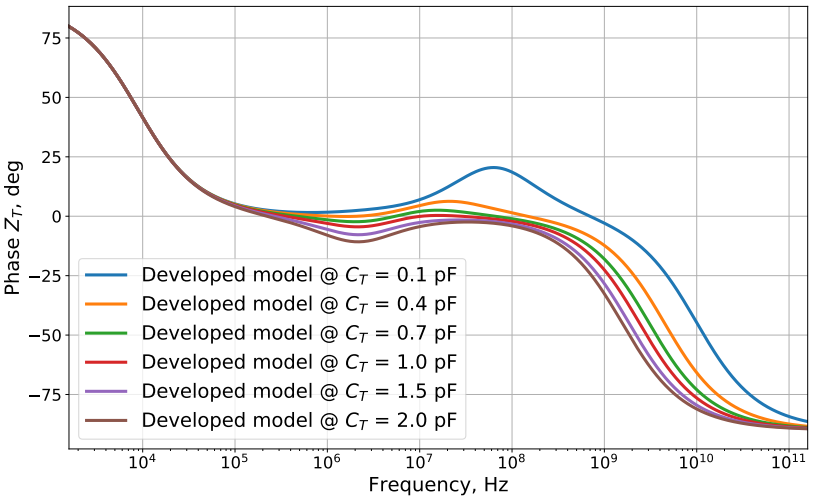

Fig. 2.9. Sensitivity of the analytically modeled phase (proposed model) to the total input capacitance with design target C_{T} = 0.7 pF and the exemplary TIA configuration of 10 kΩ

Similarly, as we have done for the gain, it may be educative to see the sensitivity of the phase for the developed analytical model with respect to the total input capacitance C_{T}. Fig. 2.9 shows the phase performance of the developed model depending on the actual value of C_{T}, where the circuit was designed assuming the value of C_{T} equal to 0.7 pF. Again, Fig. 2.10 shows the sensitivity of Shahdoost's model for the very same set of mismatched C_{T} values under the same design target. While the performance of the simpler Shahdoost model is consistent with the first-order low-pass nature of this model (single pole transfer function), where the change in C_{T} results in the trivial cut-off frequency shift in accordance

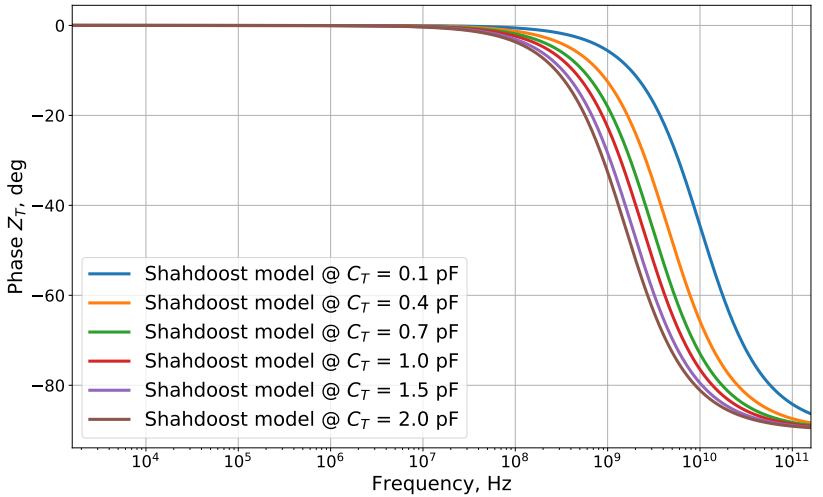

Fig. 2.10. Sensitivity of the Shahdoost model phase to the total input capacitance with design target C_{T} = 0.7 pF and the exemplary TIA configuration of 10 kΩ

to the gain response, the behavior of the proposed model is again a bit more complex. First, a two-region structure of the model is clearly visible where, similarly to the case of the gain, the impact of C_{T} becomes essential only for higher frequencies. Furthermore, for mismatch C_{T} values phase demonstrates some oscillations in mid-frequency range which is consistent to the complex underlying structure of the model. Similarly to the gain plot the corner configuration with too large C_{T} deviations cannot be properly handled by the design with target 0.7 pF.

2.3. Approximate Constant Gain Expressions

The derived detailed analytical model Z_{T} is quite complex because the complete expression for the gain includes the impact of both biasing resistors $R_{\mathrm{bias},1}$ and $R_{\mathrm{bias},2}$ along with that of the C_{C} and r_{DS5}. Design often requires a reliable approximation to the gain plateau corresponding to the mid-frequency approximation (denoted as R_{T} compared to the complete transimpedance function Z_{T}). It can be shown that for perfect biasing (both $R_{\mathrm{bias},1}$ and $R_{\mathrm{bias},2}$ approaching infinity) and ideal current source I_{SS} the original expression can be approximated as:

$$R_{\mathrm{T}} = \frac{g_{\mathrm{m},1}R_1}{1 + g_{\mathrm{m},1}R_1\frac{C_2}{C_{\mathrm{T}}+C_2}}R_2\frac{C_1}{C_{\mathrm{T}}}. \tag{2.21}$$

Here if one assumes that $g_{\mathrm{m},1}R_1C_2/(C_\mathrm{T}+C_2) \gg 1$, the expression for the mid-frequency gain R_T can be further simplified:

$$R_\mathrm{T} = \frac{C_\mathrm{T}+C_2}{C_2}R_2\frac{C_1}{C_\mathrm{T}} = \frac{C_\mathrm{T}+C_2}{C_\mathrm{T}C_2}C_1R_2. \tag{2.22}$$

Furthermore, if $C_\mathrm{T} \gg C_2$, further assumption leads to the expression we are already familiar with:

$$R_\mathrm{T} \approx \frac{C_1}{C_2}R_2. \tag{2.23}$$

As explained before, this simple expression comes under a set of assumptions. However, for the test 10 kΩ configuration the factor $g_{\mathrm{m},1}R_1C_2/\left(C_\mathrm{T}+C_2\right)$ is equal to approximately 3.2 and the assumption on this factor being much larger than one is not really fulfilled.

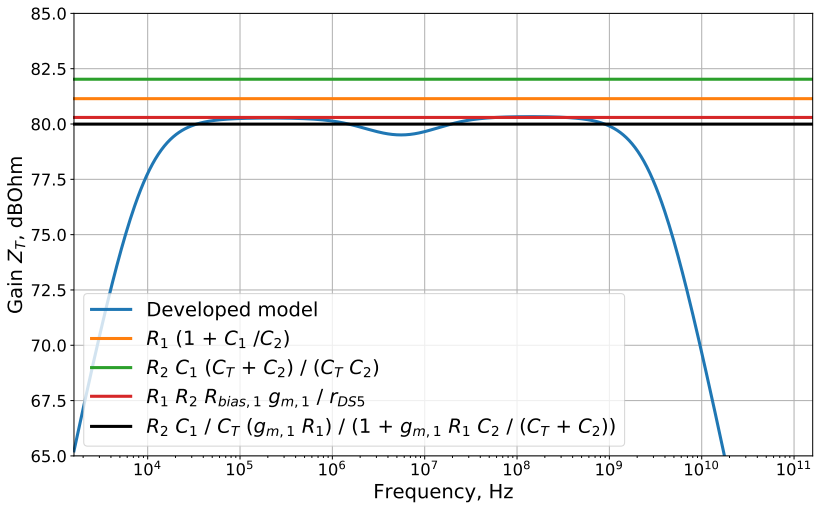

Fig. 2.11. Detailed and several constant gain approximations for the exemplary TIA configuration of 10 kΩ

Another approximation is also possible if one makes the following assumptions: $R_{\mathrm{bias},1}C_\mathrm{T} \ll 1$, $R_{\mathrm{bias},2}C_\mathrm{C} \gg 1$, $R_{\mathrm{bias},1}\left(C_\mathrm{T}+C_2\right) \ll 1$ and $C_1/g_{\mathrm{m},2} \ll 1$. Then the gain becomes:

$$R_\mathrm{T} \approx \frac{g_{\mathrm{m},1}R_1}{1+sg_{\mathrm{m},1}R_1R_{\mathrm{bias},1}C_2}R_2\frac{1+sr_{\mathrm{DS5}}C_1}{r_{\mathrm{DS5}}}R_{\mathrm{bias},1}. \tag{2.24}$$

Again further simplifications are possible as often:

$$r_{\mathrm{DS5}} C_1 \approx g_{\mathrm{m},1} R_1 R_{\mathrm{bias},1} C_2. \tag{2.25}$$

This leads to the following approximate expression for the gain plateau:

$$R_{\mathrm{T}} \approx g_{\mathrm{m},1} R_1 R_2 R_{\mathrm{bias},1} \frac{1}{r_{\mathrm{DS5}}}. \tag{2.26}$$

Obviously, which approximate gain expression to use depends on which assumptions are considered valid. An example of the detailed model and several constant gain approximations for the exemplary configuration with $R_{\mathrm{T}} \approx 10\,\mathrm{k\Omega}$ are shown in Fig. 2.11. Note that specifically for this configuration the last approximation is able to predict the gain correctly, while the approximations based on alternative set of assumptions discussed above resulted in errors of several dBΩ. What is important here is that also the famous gain expression (1.38), often cited in the literature, may not be applicable to a practical circuit designed with typical CMOS constraints.

2.4. Bandwidth

Based on the analysis above we can also compute the approximate expression for the bandwidth. This better and more realistic closed-form expression for the closed-loop -3 dB bandwidth shall also include the impact of the photodiode's capacitance. With the simplifying assumptions $C_1 \gg C_2$ and with $A_0 C_2 \gg C_{\mathrm{T}}$, the frequency response of the current gain can be approximated with (Salvia et al., 2009):

$$\frac{I_{\mathrm{out}}(s)}{I_{\mathrm{in}}(s)} = \frac{\frac{C_1}{C_2}\left(1 + \frac{s}{\frac{C_1}{C_2} A_0 BW}\right)}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}, \tag{2.27}$$

where the BW is the bandwidth of the core amplifier and:

$$\omega_0 Q = \frac{C_2 A_0 BW g_{\mathrm{m},2}}{C_1 (C_2 + C_{\mathrm{T}}) \left(BW + \frac{g_{\mathrm{m},2}}{C_1}\right)}, \tag{2.28}$$

with:

$$\omega_0^2 = \frac{C_2 A_0 BW g_{\mathrm{m},2}}{(C_2 + C_{\mathrm{T}}) C_1}. \tag{2.29}$$

This response exhibits one very high-frequency negligible zero, and two poles. If one wants to obtain a maximally flat frequency response and to ensure closed-loop stability with a safe phase margin, it is necessary to equate the real and imaginary parts of the poles. The obtained quadratic equation has two solutions and can be simplified by assuming either $BW^2 \gg (g_{\mathrm{m},2}/C_1)^2$ or $BW^2 \ll (g_{\mathrm{m},2}/C_1)^2$. For the first case it may be shown that:

$$BW = \frac{2A_0C_2}{C_2 + C_{\mathrm{T}}} \frac{g_{\mathrm{m},2}}{C_1}, \tag{2.30}$$

while for the second case:

$$BW = \frac{C_2 + C_{\mathrm{T}}}{2A_0C_2} \frac{g_{\mathrm{m},2}}{C_1}. \tag{2.31}$$

Here we choose to design for the first case in order to minimize the current through M_2. Furthermore, this case also reduces the noise contribution of M_2 and allows for maximum R_2. With the closed-loop -3 dB bandwidth as:

$$BW_{-3\mathrm{dB}} = \frac{BW}{\sqrt{2}}, \tag{2.32}$$

one finally gets for the CS-based core amplifier:

$$BW_{-3\mathrm{dB}} = \frac{1}{\sqrt{2}} \frac{2g_{\mathrm{m},2}C_2A_0}{2\pi C_1 (C_2 + C_{\mathrm{T}})} = \frac{1}{\sqrt{2}} \frac{g_{\mathrm{m},2}C_2g_{\mathrm{m},1}R_1}{\pi C_1 (C_2 + C_{\mathrm{T}})}. \tag{2.33}$$

As we have seen in Fig. 2.4, the actual bandwidth is likely to be a bit larger than the one based on using simplifying approximations. Unfortunately, the final expressions for Z_{T} become too complex for an easy interpretable close-form solution to be found.

2.5. Fixed-Gain Configuration With Optimized Biasing

Let us consider the biasing for M_2 transistor. A special challenge in terms of an area-efficient design comes due to the requirement to have a low cut-off frequency of 100 kHz. The signal at the gate of the source follower transistor comes through the capacitance C_{C}. If the biasing resistor $R_{\mathrm{bias},2}$ is low, the signal will almost be short-circuited. Thus, for the DC operation of the transistor M_2 we need to have a bias voltage, but this biasing should be provided through a large resistance. As a result, the combination of the C_{C} and $R_{\mathrm{bias},2}$ shall operate as a low-pass filter

with relatively low cut-off frequency. The combination of the current source I_{DC} along with $M_{2\mathrm{B}}$ and R_{S} can be considered as a voltage source. This is connected in series with our required $R_{\mathrm{bias},2}$ and shall provide the required voltage $V_{\mathrm{g}2}$. By matching the current source I_{DC} to the resistance R_{S} and the dimensions of M_2 we can define the voltage at the source of $M_{2\mathrm{B}}$ ($V_{\mathrm{s}3}$) to be equal to the one of M_2 ($V_{\mathrm{s}2}$) we want to bias. If there is no signal in TIA, the voltage $V_{\mathrm{s}2}$ is a DC voltage which is defined by the product of current sourced by I_{DC} times the R_{S}. Then the voltage at the gate of $M_{2\mathrm{B}}$ is approximately the sum of our defined $V_{\mathrm{s}2}$, the threshold voltage V_{th} and the effective voltage V_{eff} and is equal to the our intended biasing voltage $V_{\mathrm{g}2}$ at the gate of M_2. If the target transistor M_2 and the current through it are scaled proportionally to the voltage source transistor $M_{2\mathrm{B}}$, then the threshold voltages for both transistors are the same resulting in our target operating $V_{\mathrm{s}2}$. This DC voltage must be chosen in such a way that the imposed signal has sufficient swing capability and is not clipped neither from below nor from above. When designing the current source I_{SS}, the voltage at the gate of the transistor M_5:

$$V_{\mathrm{g}5} = V_{\mathrm{th}} + V_{\mathrm{eff}}, \tag{2.34}$$

where the effective voltage V_{eff} is approximately the saturation voltage over M_5. With the $V_{\mathrm{g}2}$ of around 1.2 V, the value of $V_{\mathrm{s}2}$ becomes effectively around 600 mV which allows a signal swing of at least 400 mV in both directions (800 mV total).

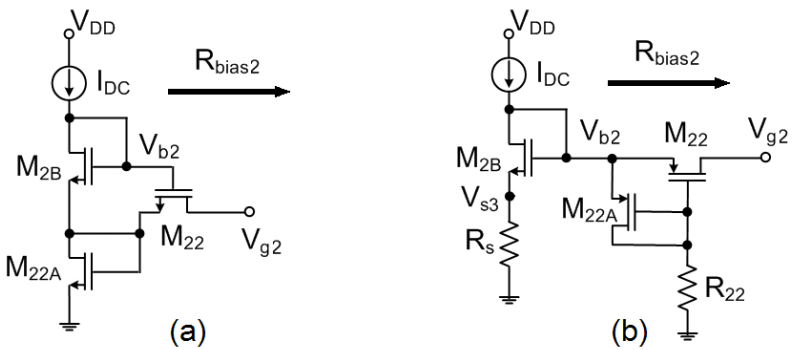

Fig. 2.12. Original NMOS-based implementation of the biasing circuit (a) and modified PMOS-based implementation (b). Corresponding parasitic capacitances which make the circuit to perform as a low-pass filter are not shown

In the previously discussed implementation one shall place resistors $R_{\mathrm{bias},1}$ and $R_{\mathrm{bias},2}$ at the corresponding gates of M_1 and M_2 to provide correspondingly $V_{\mathrm{g}1}$ of around 0.7 V and $V_{\mathrm{g}2}$ of around 1.2 V. A further complication comes from the fact that we also want to minimize the parasitic capacitance. For the configu-

ration with a gain of R_{T} = 10 kΩ the $R_{\mathrm{bias},1}$ may be in the range 16 kΩ -20 kΩ and a straightforward implementation with bias resistor can be applied for biasing M_1 due to a negligible impact on the total area of the circuit. This implementation, however, can be hardly used for $V_{\mathrm{g}2}$ as the value of the resistance becomes in MΩ range and it may prohibit a practical area-efficient implementation of the circuit.

An attempt to address similar problem had been already demonstrated before in (Shahdoost et al., 2016) and is shown in Fig. 2.12 (a), where a biasing circuit formed by three NMOS transistors was suggested for a design running from 2.2 V supply (parasitic capacitances, which make the circuit to perform as a low-pass filter, are not shown). This three-transistor topology plays the role of a very large resistor while occupying considerably less silicon area compared to using a regular resistance on the chip with the same resistance value. In this bias network the biased transistors (e.g., M_1 or M_2 in our design) and $M_{22\mathrm{A}}$ form a current mirror. I_{DC} and $M_{2\mathrm{B}}$ also define the on-resistance of M_{22}, which provides large resistance for isolation of the signal path from the low impedance introduced by $M_{22\mathrm{A}}$. Unfortunately, the proposed approach, while running from 2.2 V supply, is hardly applicable in the present design with 1.8 V supply due to voltage headroom problem.

In order to mitigate the problem of an area-efficient design with $R_{\mathrm{bias},2}$, we suggest an alternative approach for $V_{\mathrm{g}2}$ using two PMOS devices M_{22} and $M_{22\mathrm{A}}$ as shown in Fig. 2.12 (b). The proposed approach addresses the NMOS problem with the voltage headroom as while $V_{\mathrm{DD}} - V_{\mathrm{g}2}$ is not sufficient for proper operation of NMOS devices, the voltage difference $V_{\mathrm{g}2} - V_{\mathrm{GND}}$ provides enough voltage for PMOS-based implementation. Here one takes corresponding $L_{22} = L_{22\mathrm{A}}$ and $W_{22} = 1/N \cdot W_{22\mathrm{A}}$ constrained with $V_{\mathrm{eff},22} = V_{\mathrm{eff},22\mathrm{A}}$. The equivalent bias resistance for the configuration shown becomes:

$$R_{\mathrm{bias},2} = R_{\mathrm{DS},22} = \frac{1}{\sqrt{2\beta_{\mathrm{P}} I_{22\mathrm{A}}}} \frac{L_{22}\sqrt{W_{22\mathrm{A}}}}{W_{22}\sqrt{L_{22\mathrm{A}}}} = \frac{N}{\sqrt{2\beta_{\mathrm{P}} I_{22\mathrm{A}}}} \frac{\sqrt{L_{22}}}{\sqrt{W_{22}}}, \qquad (2.35)$$

where L_{22}, $L_{22\mathrm{A}}$ and W_{22}, $W_{22\mathrm{A}}$ are the corresponding dimensions of the M_{22} and $M_{22\mathrm{A}}$ and β_{P} is the transconductance parameter for PMOS device. In this new design, the transistor $M_{22\mathrm{A}}$ is set to be 10 times bigger than M_{22}. While the M_{22} operates in linear mode, the $M_{22\mathrm{A}}$ ensures a stable voltage $V_{\mathrm{g}2}$ with resistor R_{22} used to limit the current $I_{22\mathrm{A}}$ to just a few μA. Note that if the current is added via R_{22}, the same current has to be removed from I_{DC} for $M_{2\mathrm{B}}$ transistor. The design results in 0.8 V at the gate of both transistors with $V_{\mathrm{g}2}$ stable around 1.2 V. Finally, an additional resistor R_{S} is employed to add an extra voltage and the current source at $V_{\mathrm{s}2}$ is implemented with a carefully designed current mirror.

2.6. Programmable-Gain Configuration

An efficient implementation of the TIA for practical low-cost OTDR instruments results in the necessity to develop the circuit supporting programmable-gain configuration. This is caused by the inherent relationship between the responsivity of the PD/APD and the requirement for the dynamic range and gain of the instrument, as we discussed in Chapter 1. A large gain of the PD results in an increased amount of noise generated in the circuit, while as the gain of TIA increases, the bandwidth correspondingly decreases and a PD with a smaller gain can be used. Thus, with the TIA supporting a range of gain-bandwidth configurations, one is able to effectively use the same circuit with different PDs enabling varying operating modes for the same device, including support for very weak optical signals and short optical pulses.

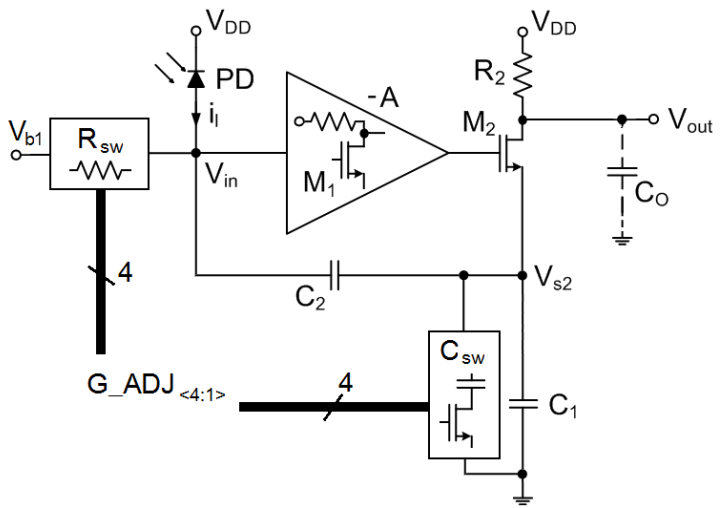

Fig. 2.13. Concept for a programmable-gain capacitive feedback TIA. The core CS-based voltage amplifier is only schematically sketched and ancillary components are omitted for simplicity

There are several general concepts on how to get a programmable-gain configuration for the given TIA. One of the simplest options would be to implement TIA merely as a current buffer and add an additional voltage gain stage with a variable gain. However, as we have already commented before, if possible, one shall opt to use less active components and less stages to reduce both the noise and the power consumption of the complete circuit, and the requirement for an additional gain stage does not benefit the overall performance of the design. This is especially important as the fixed-gain design demonstrated above confirms that we can achieve

the required gain-bandwidth product without any additional post-amplifier and we may keep the structure of the TIA maximally similar to the proposed fixed-gain version. Therefore, we select an alternative approach, where the gain variation is implemented within the main TIA block without additional amplification stages (see Mekky et al., (2013) for the discussion on possible alternatives).

The concept for the programmable-gain configuration capacitive feedback TIA is shown in Fig. 2.13 and employs a simultaneous adjustment of M_1 (input transistor within the core CS-based amplifier) biasing network and the feedback capacitor C_1. The modifications necessary for programmable-gain functionality are elaborated for $R_{\mathrm{bias},1}$ in Fig. 2.14 and for C_1 in Fig. 2.15 correspondingly. The proposed approach also allows an independent tuning for low- and high-frequency ranges of the pass-band and significantly simplifies the design process when compared to one parameter approach where, for example, the resistor R_2 is adjusted.

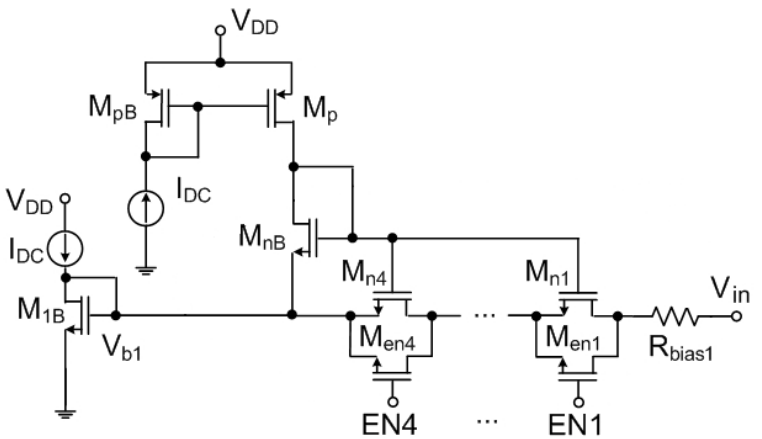

Fig. 2.14. Implementation of $R_{\mathrm{bias},1}$ switch for programmable-gain capacitive feedback TIA

A parallel connection of the capacitance increments as required for each gain configuration forms the overall capacitance C_1. However, only the upper part of the amplifier pass-band is addressed with the adjustment of C_1 via its coupling to the gain of the second stage. Here the tuning of $R_{\mathrm{bias},1}$ implements the missing additional control knob for the lower part of the pass-band and allows an independent adjustment of the gain to that implemented with C_1. Based on the general gain expression elaborated before, the overall gain depends on both C_2 and C_1. In order to avoid redundant adjustments we suggest C_2 to be kept constant and it shall be selected very small (e.g., several times larger than the minimum capacitance which can be implemented with the given technology).

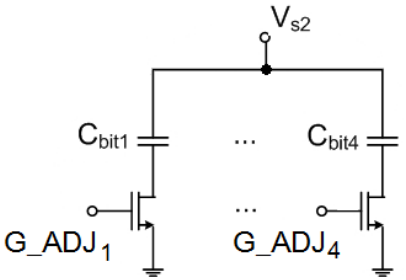

Fig. 2.15. Implementation of C_1 switch for programmable-gain capacitive feedback TIA

The design as above provides us with an extremely simple mechanism for extending the fixed-gain implementation to the one with discretely controlled gain:

1. Using the methodology from previous sections, design a capacitive feedback TIA with PMOS-based biasing circuits for a base gain (the lowest gain, e.g. mid-frequency gain R_{T} of 10 kΩ as in the proposed design).
2. For the required gain R_{T}^* (or each gain in the set of gains sorted in ascending order) compute the new values of the feedback capacitance C_1^*:

$$C_1^* = \frac{R_{\mathrm{T}}^*}{R_{\mathrm{T}}} C_1, \tag{2.36}$$

   and correspondingly the biasing resistor $R_{\mathrm{bias},1}^*$:

$$R_{\mathrm{bias},1}^* = \frac{R_{\mathrm{T}}^*}{R_{\mathrm{T}}} R_{\mathrm{bias},1}. \tag{2.37}$$

3. Compute the required increment of the feedback capacitance ΔC_1:

$$\Delta C_1 = C_1^* - C_1, \tag{2.38}$$

   and, correspondingly, the increment in the bias resistor $\Delta R_{\mathrm{bias},1}$:

$$\Delta R_{\mathrm{bias},1} = R_{\mathrm{bias},1}^* - R_{\mathrm{bias},1}, \tag{2.39}$$

   and add the required components for $R_{\mathrm{bias},1}$ as shown in Fig. 2.14 and for C_1 as shown in Fig. 2.15.
4. Replace $R_{\mathrm{T}}^* \to R_{\mathrm{T}}$, $R_{\mathrm{bias},1}^* \to R_{\mathrm{bias},1}$, $C_1^* \to C_1$ and repeat the process for the rest of the gains if needed.

Obviously, the methodology results in a very simple linear scaling of the two tuning parameters by the required gain ratio with respect to the base gain for which the

original TIA was designed. Note that the method still implies that the amplifier for the base gain is correctly calculated. Therefore, if the original amplifier is designed using simplified expressions, a corresponding error in gain will be propagated by the methodology above. However, due to linearity of the scaling methodology, even such gross errors can be easily tuned out by a simultaneous adjustment of C_1 and $R_{\mathrm{bias},1}$. This confirms the universality of the proposed scheme as it can be adopted even for designs based on very rough gain approximations.

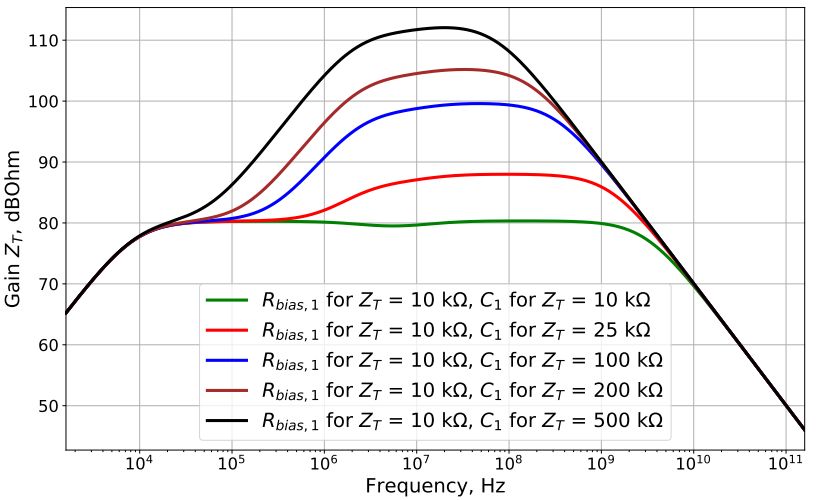

Fig. 2.16. Gain performance of developed model when changing only C_1 while keeping $R_{\mathrm{bias},1}$ constant for base TIA configuration 10 kΩ

As we explained before, the proposed double control scheme for programmable-gain configuration allows an independent adjustment of the TIA performance in low- and high-frequency ranges. A practical impact of this adjustment is shown in Fig. 2.16 for the developed detailed model, where the value of C_1 is adjusted according to the proposed programmable-gain scheme, while the value for $R_{\mathrm{bias},1}$ is kept equal to the one which is used for the baseline gain configuration of 10 kΩ. We see that the gain in the mid- and high-frequency range is adjusted, while the performance close to the lower cut-off frequency remains the same. A complementary performance is demonstrated in Fig. 2.17 for the very same model, where the value of $R_{\mathrm{bias},1}$ is adjusted according to the proposed scheme while C_1 is kept constant as computed for the base configuration of R_{T} = 10 kΩ. Here, differently, the gain in low-frequency range is adjusted, while the behavior in mid- and high-frequency range remains intact. This confirms the desired complementary properties of the suggested programmable-gain scheme, because a relatively flat pass-band can be obtained by an independent tuning of both values. The results of the model when

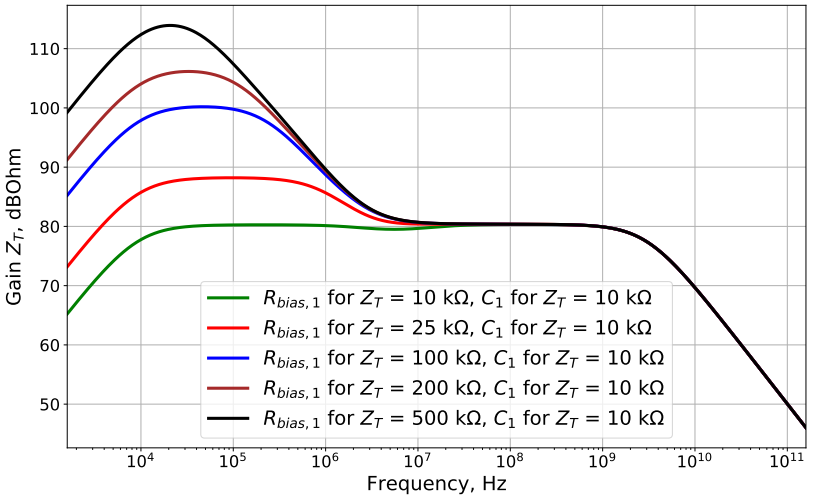

Fig. 2.17. Gain performance of developed model when changing only $R_{\mathrm{bias},1}$ while keeping C_1 constant for base TIA configuration 10 kΩ

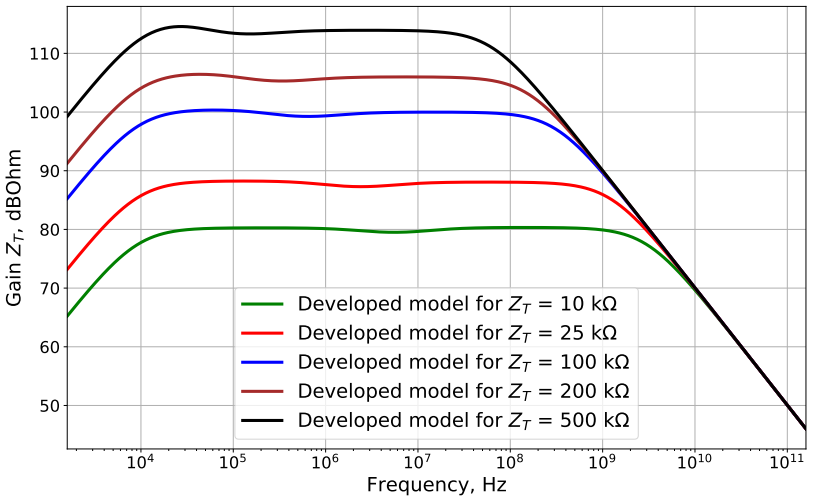

Fig. 2.18. Gain performance of developed model when changing both $R_{\mathrm{bias},1}$ and C_1 for desired five gain configurations

both C_1 and $R_{\mathrm{bias},1}$ are simultaneously adjusted following the procedure as described above (e.g. the proposed programmable-gain concept itself), are presented in Fig. 2.18. Small artifacts for large gain values in the low-frequency part of the plateau are likely to be caused by insufficient tuning efforts for the circuit parameters.

2.7. Noise Model

The input-referred noise current $i_{\mathrm{n,TIA}}$ is an important parameter when characterizing the TIA design, as it determines the overall sensitivity of the circuit. Below we show how the noise model can be derived for the developed circuit and which noise sources play the most important role. As we have argued before, one of the major advantages of the capacitive feedback TIA is that the feedback network itself is noiseless and contributes no noise as opposed to the traditional resistive feedback network. Furthermore, the current thermal noise due R_2 will be suppressed when divided by the current gain of the circuit. As we will see, this only holds for the circuit operating under ideal conditions and additional noise sources may appear due to imperfections in biasing circuits, current mirrors, etc.

2.7.1. Resistor Noises

A general noise component due to resistor R is a thermal noise and is modeled by a voltage source in series with the resistor or a current source in parallel with resistor. The noise is generated by the thermal agitation of the charge carriers that occurs inside any electrical conductor. For the noise representation as the voltage source one gets:

$$\frac{\overline{v_{\mathrm{nr1}}^2}}{\Delta f} = 4\mathrm{k_B}TR. \tag{2.40}$$

Note that the noise voltage is proportional to that resistor R and to the absolute temperature, but does not depend on the actual current flowing through the resistor, and the noise is white. The equivalent noise current becomes:

$$\frac{\overline{i_{\mathrm{nr1}}^2}}{\Delta f} = \frac{4\mathrm{k_B}T}{R}. \tag{2.41}$$

There are several sources for the resistor noise which we may need to consider. First, recall that our first biasing circuit is resistive and we shall not assume the noise due to the biasing resistor $R_{\mathrm{bias,1}}$ to be negligible. On the other hand, the current thermal noise due to R_2 will be suppressed by the approximate gain due to capacitive feedback:

$$\frac{\overline{i_{\mathrm{nr2}}^2}}{\Delta f} = \frac{4\mathrm{k_B}TR_2}{R_{\mathrm{T}}^2} \approx \frac{4\mathrm{k_B}T}{R_2\left(1+\frac{C_1}{C_2}\right)^2}. \tag{2.42}$$

The approximation above may not be applied in general case as we have seen in previous sections. However, in all the cases the noise contribution of R_2 is decreased

by a very significant factor for the frequencies where the gain is significant, i.e. exactly within the bandwidth of the TIA. Thus, the final thermal noise consists correspondingly of two terms: noise contribution due to $R_{\mathrm{bias},1}$ in biasing circuit for M_1 and contribution due to R_2 with the gain down-scaling:

$$\frac{\overline{i_{\mathrm{nr}}^2}}{\Delta f} = \frac{\overline{i_{\mathrm{nr1}}^2}}{\Delta f} + \frac{\overline{i_{\mathrm{nr2}}^2}}{\Delta f} = \frac{4\mathrm{k_B}T}{R_{\mathrm{bias},1}} + \frac{4\mathrm{k_B}TR_2}{R_{\mathrm{T}}^2}. \tag{2.43}$$

Note that often the modeling of capacitive feedback TIA ignores the non-perfect biasing of practical circuits and considers solely the down-scaled noise contribution from R_2.

2.7.2. Channel Thermal Noise

When it comes to noise in MOS transistor, there are several different noise sources to consider. The two most important noise contributions are the thermal noise in the channel and $1/f$ noise. Further noise sources are typically considered as relatively minor and include the noise due to the distributed substrate resistance, noise in the resistive poly gate and the shot noise associated with the leakage current of the drain source reverse diodes. For typical scenarios only the first two components of the MOS noise can be taken into account. The rest of the noise sources may be considered for very low-noise application and we will ignore them while deriving our TIA noise model.

A MOSFET has an inverse resistive channel between the drain and the source when operating in normal mode. In the extreme case, when the $V_{DS} = 0$, the channel can be treated as a homogeneous resistor with the noise in the channel:

$$\frac{\overline{i_{\mathrm{nt}}^2}}{\Delta f} = 4\mathrm{k_B}Tg_0, \tag{2.44}$$

where g_0 is the channel conductance at zero drain-source voltage. In practice, however, $V_{\mathrm{DS}} \neq 0$ and therefore the channel is more conductive nearby the source compared to the drain, and the channel cannot be modeled anymore as a homogeneous resistor. As a result, the numerical integration along the whole channel has to be performed with the noise calculated in every small part Δx of the channel. This integral is hard to solve and in short one typically writes:

$$\frac{\overline{i_{\mathrm{nt}}^2}}{\Delta f} = 4\mathrm{k_B}T\gamma g_{\mathrm{d0}}, \tag{2.45}$$

where the factor γ is a complex function of the basic transistor parameters and

bias conditions, which has to be found numerically. For modern CMOS processes the factor γ is typically between 0.67 for long channel devices in saturation and 2 or even higher for sub-micron devices. Note that in the expression above g_{d0} is zero-bias drain conductance. However, the thermal noise of the channel when referred to input shall be represented by a voltage source in series with gate. Then the voltage spectral density becomes:

$$\frac{\overline{v_{\mathrm{nt}'}^2}}{\Delta f} = \frac{8}{3}\frac{\mathrm{k_B}Tg_{\mathrm{d0}}}{g_{\mathrm{m}}^2}. \tag{2.46}$$

Often one takes g_{d0} equal to the transconductance of the transistor in saturation g_{m} which gives us a bit simpler equation:

$$\frac{\overline{v_{\mathrm{nt}'}^2}}{\Delta f} \approx \frac{8}{3}\frac{\mathrm{k_B}T}{g_{\mathrm{m}}}. \tag{2.47}$$

For our presented design we shall consider this noise component for transistor M_1 with $g_{\mathrm{m},1}$.

2.7.3. Flicker Noise

When charge carriers move at the interface, the random charge trapping by the energy states introduces noise into the drain current which is called flicker noise. Depending on the impurities of the oxide-silicon interface, this noise may vary from process to process. Flicker noise is modeled by a current source across the drain and is expressed with the following current spectral density:

$$\frac{\overline{i_{\mathrm{nf}}^2}}{\Delta f} = \frac{K_{\mathrm{f}}}{f}\frac{g_{\mathrm{m}}^2}{C_{\mathrm{ox}}WL}, \tag{2.48}$$

where K_f is the flicker noise constant, W and L are correspondingly the width and the length of the channel. When referred to input, the noise is represented by a voltage source between gate and source. The voltage spectral density of this voltage source is:

$$\frac{\overline{v_{\mathrm{nf}}^2}}{\Delta f} = \frac{K_{\mathrm{f}}}{f}\frac{1}{C_{\mathrm{ox}}WL}, \tag{2.49}$$

where K_{f} is a device-specific constant and W, L are the effective width and length of the MOS device. Note that the value of K_{f} of PMOS devices is an order lower than that of NMOS devices. Therefore, PMOS devices are believed to exhibit less flicker noise than NMOS devices. Flicker noise has inverse dependency on frequency, so it is also often called $1/f$ noise (yet another name of pink noise). Simi-

lar to the case of the channel thermal noise, this noise shall be again considered at least for the input transistor M_1.

As flicker noise reduces with increasing frequency, at some point it starts falling much below the thermal noise. The frequency at which flicker noise is equal to thermal noise is called the corner frequency f_{C} of flicker noise:

$$\frac{\overline{i_{\mathrm{nt}}^2\left(f_{\mathrm{C}}\right)}}{\Delta f} = \frac{\overline{i_{\mathrm{nf}}^2\left(f_{\mathrm{C}}\right)}}{\Delta f} \Rightarrow 4\mathrm{k_B}T\gamma g_{\mathrm{m}} = \frac{K_{\mathrm{f}}}{f}\frac{g_{\mathrm{m}}^2}{C_{\mathrm{ox}}WL} \tag{2.50}$$

Solving the equation above for f_{C} we get:

$$f_{\mathrm{C}} = \frac{K_{\mathrm{f}}}{\gamma}\frac{g_{\mathrm{m}}}{4\mathrm{k_B}TC_{\mathrm{ox}}WL}. \tag{2.51}$$

If we substitute:

$$\omega_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{C_{\mathrm{s}}} \approx \frac{g_{\mathrm{m}}}{C_{\mathrm{ox}}WL}, \tag{2.52}$$

we finally get:

$$f_{\mathrm{C}} = \frac{K_{\mathrm{f}}}{\gamma}\frac{\omega_T}{4\mathrm{k_B}T}. \tag{2.53}$$

Obviously, the flicker noise is directly proportional to technology scaling ω_{T}: when it increases, the flicker noise also. Though flicker noise is small at RF frequencies, its effect may be considerable in mixers and oscillators due to non-linearities or time variance of those circuits.

2.7.4. Combined Noise Model

Considering the terms described above:

$$\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} = \frac{\overline{i_{\mathrm{nr}}^2}}{\Delta f} + \frac{1}{Z_{\mathrm{IN,eff}}^2}\left(\frac{\overline{v_{\mathrm{nt'}}^2}}{\Delta f} + \frac{\overline{v_{\mathrm{nf}}^2}}{\Delta f}\right). \tag{2.54}$$

After substituting the expressions from previous sections and noticing the thermal noises on both the bias resistance $R_{\mathrm{bias,1}}$ and R_2, we get:

$$\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} = \frac{4\mathrm{k_B}T}{R_{\mathrm{bias,1}}} + \frac{4\mathrm{k_B}TR_2}{Z_{\mathrm{T}}^2} + \frac{1}{Z_{\mathrm{IN,eff}}^2}\left(\frac{8}{3}\frac{\mathrm{k_B}T}{g_{\mathrm{m,1}}} + \frac{K_{\mathrm{f}}}{f}\frac{1}{C_{\mathrm{ox}}WL}\right). \tag{2.55}$$

Although the expression above provides a fairly good approximation of the noise in mid- and high-frequency range as well as captures typical $1/f$ flicker noise behavior of M_1, practical circuit implementation with the current source I_{SS} im-

plemented via M_5 may introduce an additional noise source which is often ignored with approximate noise modeling. Here, the flicker noise of M_5 at the node V_{s2} becomes an additional drain current of M_2 and after multiplication with R_2 becomes the voltage noise at the output of our amplifier (here, for the noise consideration we ignore the output buffer). However, the ratio of the output voltage to the input current is exactly the transimpedance gain Z_{T} we have computed in previous sections:

$$Z_{\mathrm{T}} = \frac{V_{\mathrm{out1}}}{I_{\mathrm{in}}}.$$

Thus, by dividing the noise current gain R_2 by Z_{T} we obtain the transfer function of the M_5 noise at the node V_{s2} to the input current noise:

$$G_{\mathrm{M5}} = \frac{R_2}{Z_{\mathrm{T}}}. \tag{2.56}$$

The combined noise model including the contribution from M_5 can be written as:

$$\begin{aligned}\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} &= \frac{4\mathrm{k_B}T}{R_{\mathrm{bias,1}}} + \frac{4\mathrm{k_B}TR_2}{Z_{\mathrm{T}}^2} + \frac{1}{Z_{\mathrm{IN,eff}}^2}\left(\frac{8}{3}\frac{\mathrm{k_B}T}{g_{\mathrm{m,1}}} + \frac{K_{\mathrm{f,M1}}}{f}\frac{1}{C_{\mathrm{ox}}W_{\mathrm{M1}}L_{\mathrm{M1}}}\right)\\ &+ G_{\mathrm{M5}}^2\frac{K_{\mathrm{f,M5}}}{f}\frac{1}{C_{\mathrm{ox}}W_{\mathrm{M5}}L_{\mathrm{M5}}}.\end{aligned} \tag{2.57}$$

Note that for simplicity we only consider the $1/f$ noise of M_5 and ignore the thermal channel noise. Recall also from the discussion of the gain that the input impedance:

$$Z_{\mathrm{IN}} = \frac{R_{\mathrm{bias,1}}}{1 + sR_{\mathrm{bias,1}}C_{\mathrm{T}}}. \tag{2.58}$$

For noise, however, we consider a so-called effective input impedance:

$$Z_{\mathrm{IN,eff}} = \frac{R_{\mathrm{bias,1}}}{1 + sR_{\mathrm{bias,1}}C_{\mathrm{T,eff}}} = \frac{R_{\mathrm{bias,1}}}{1 + sR_{\mathrm{bias,1}}\left(C_{\mathrm{T}} + C_{\mathrm{M1}} + C_{\mathrm{in2vs}}\right)}, \tag{2.59}$$

where the input capacitance is inflated with that due to transistor M_1 and input capacitance to ground. Due to small contribution of R_2 the overall input-referred noise density can be effectively approximated as following for mid- and high-frequency ranges:

$$\begin{aligned}\frac{\overline{i_{\mathrm{n}}^2}}{\Delta f} &\approx \frac{4\mathrm{k_B}T}{R_{\mathrm{bias,1}}} + \frac{1}{Z_{\mathrm{IN,eff}}^2}\left(\frac{8}{3}\frac{\mathrm{k_B}T}{g_{\mathrm{m,1}}} + \frac{K_{\mathrm{f,M1}}}{fC_{\mathrm{ox}}W_{\mathrm{M1}}L_{\mathrm{M1}}}\right)\\ &+ \frac{K_{f,M5}G_{\mathrm{M5}}^2}{fC_{\mathrm{ox}}W_{\mathrm{M5}}L_{\mathrm{M5}}}.\end{aligned} \tag{2.60}$$

Let us consider incrementally the impact of each noise component in our final model. To make the analysis more intuitive, we plot the results for all five gain configurations in order to observe also an impact of both increased C_1 and $R_{\mathrm{bias},1}$. Fig. 2.19 shows the noise component:

$$\frac{\overline{i_{\mathrm{nt}'}^2}}{\Delta f} \approx \frac{1}{Z_{\mathrm{IN,eff}}^2} \frac{8}{3} \frac{\mathrm{k_B}T}{g_{\mathrm{m},1}}, \tag{2.61}$$

for all five programmable-gain configurations and $T = 298.15\mathrm{K}$. This noise component defines the voltage noise at the gate of the transistor M_1 and is mostly responsible for the high-frequency noise. One can also compute the M_1 noise component due to the $R_{\mathrm{bias},1}$ which gives us the current density of around 0.02 pA/$\sqrt{\mathrm{Hz}}$ for the base gain configuration of 10 kΩ. Thus the transistor noise on the bias resistor is below our requirement of 5 pA/$\sqrt{\mathrm{Hz}}$. Recall that in programmable-gain configuration the value of $R_{\mathrm{bias},1}$ is different depending on the gain so that the effective input impedance is also automatically lower for larger gains due to larger values of bias resistance. Although this component explains fairly well the noise performance of TIA in high-frequency range, the predicted noise levels in the mid- and low-frequency range shall be investigated further.

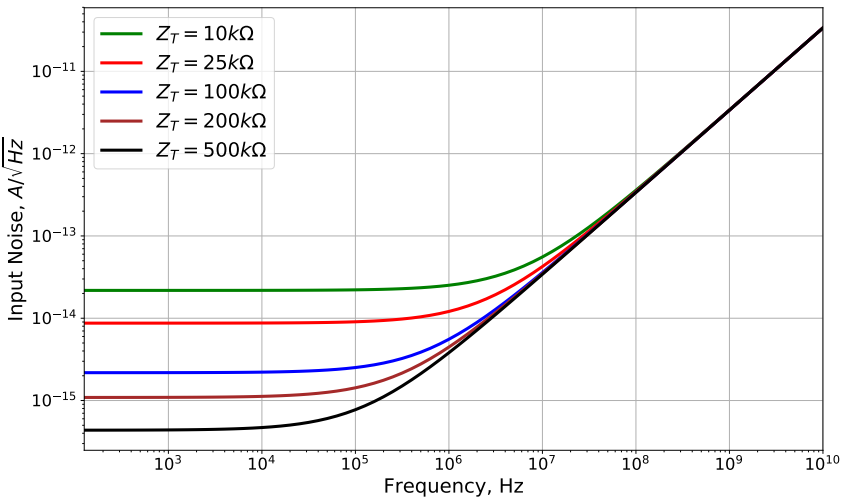

Fig. 2.19. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component only

The results of our proposed noise model for both M_1 thermal noise and the noise component due to $R_{\text{bias},1}$:

$$\frac{\overline{i^2_{\text{nt}'}}}{\Delta f} + \frac{\overline{i^2_{\text{nr1}}}}{\Delta f} \approx \frac{1}{Z^2_{\text{IN,eff}}} \frac{8}{3} \frac{\text{k}_\text{B}T}{g_{\text{m},1}} + \frac{4\text{k}_\text{B}T}{R_{\text{bias},1}}, \tag{2.62}$$

are shown in Fig. 2.20. Clearly, the white noise due to the bias resistor dominates in mid- and low-frequency range and pulls up significantly the noise to the level of approximately 1 pA/$\sqrt{\text{Hz}}$ for the base R_T configuration with 10 kΩ gain.

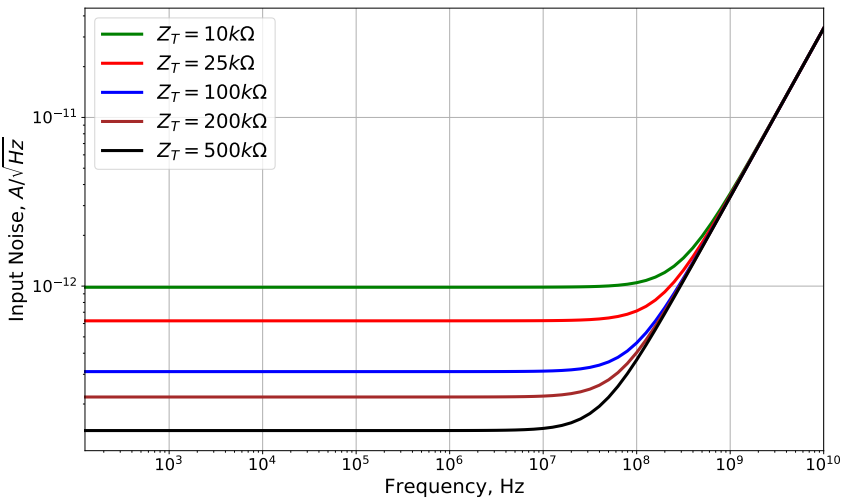

Fig. 2.20. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component and noise due to $R_{\text{bias},1}$

Next we extend the noise model with the noise component due to R_2:

$$\frac{\overline{i^2_{\text{nt}'}}}{\Delta f} + \frac{\overline{i^2_{\text{nr1}}}}{\Delta f} + \frac{\overline{i^2_{nr2}}}{\Delta f} \approx \frac{1}{Z^2_{\text{in,eff}}} \frac{8}{3} \frac{\text{k}_\text{B}T}{g_{\text{m},1}} + \frac{4\text{k}_\text{B}T}{R_{\text{bias},1}} + \frac{4\text{k}_\text{B}TR_2}{Z^2_\text{T}}. \tag{2.63}$$

The results are shown in Fig. 2.21 where we expected to see the white resistor noise added to our previous results. The observed result is a bit unexpected. As we have discussed before, the noise component $\overline{i^2_{\text{nr2}}}$ in literature is typically approximated as:

$$\frac{\overline{i^2_{\text{nr1}}}}{\Delta f} \approx \frac{4\text{k}_\text{B}T}{R_2 \left(1 + \frac{C_1}{C_2}\right)^2}. \tag{2.64}$$

This model stands for the white noise (constant PSD) and this value is very small when compared to the noise floor set by the noise of $R_{\mathrm{bias},1}$. However, this simplified expression is only valid if we assume constant gain of the TIA down to the DC, where for a typical TIA configuration, the noise due to R_2 would be about two orders of magnitude smaller than the noise of $R_{\mathrm{bias},1}$ (this ratio would hold for other gain configurations due to the simultaneous $R_{\mathrm{bias},1}$ noise reduction). As we have demonstrated in previous sections, the assumption on constant gain is not true due to the band-pass behavior of the proposed circuit, and the noise of R_2 gets amplified for very low frequencies. Note that this effect was completely ignored in the works of other authors.

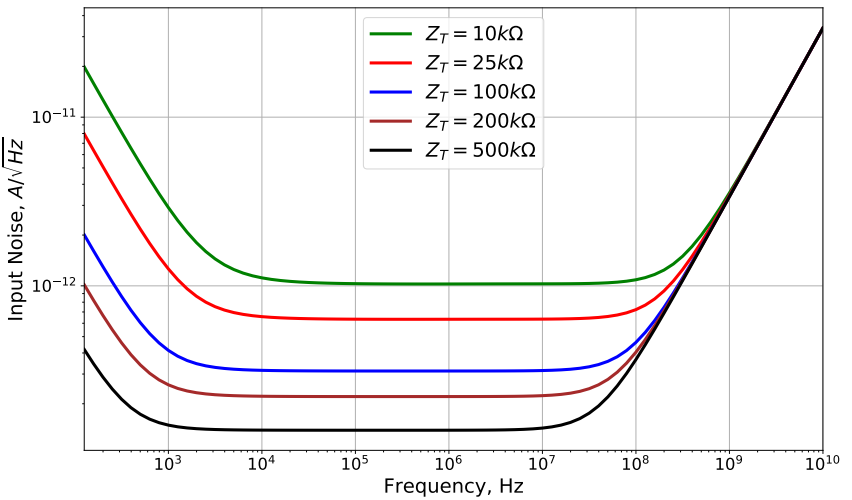

Fig. 2.21. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component and noises due to $R_{\mathrm{bias},1}$ and R_2

Now let us also add a flicker noise component for the input transistor M_1:

$$\frac{\overline{i_{\mathrm{nf}}^2}}{\Delta f} = \frac{1}{Z_{\mathrm{in,eff}}^2} \frac{K_{\mathrm{f}}}{f} \frac{1}{C_{\mathrm{ox}} W L}. \tag{2.65}$$

The parameter $K_{\mathrm{f}}/C_{\mathrm{ox}}WL$ for M_1 gives us around 10 µA. The performance of our developed model with four noise components is shown in Fig. 2.22. We can clearly see the impact of the flicker noise component in the transition region between mid- and high frequencies. Unfortunately, the famous $1/f$ noise gets hidden behind the shaped noise of R_2. The $1/f$ noise due to its square-root dependency in PSD gives the 10 dB/decade drop which is only partially seen in the transition region.

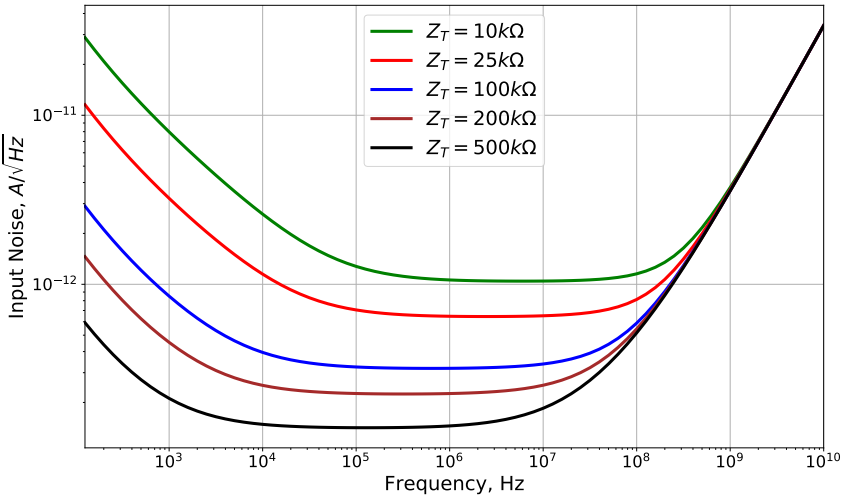

Fig. 2.22. Analytically calculated input-referred noise model for programmable-gain configuration with M_1 thermal noise component, noises due to $R_{\mathrm{bias},1}$, R_2 and flicker noise on M_1

Finally, let us complete the noise model by adding the last component describing the flicker noise caused by M_5 which is shown in Fig. 2.23. Clearly, this is just a scaled inverse of our designed transimpedance function Z_{T}. From the design it becomes obvious that more noise will be passed for extremely low and high frequencies.

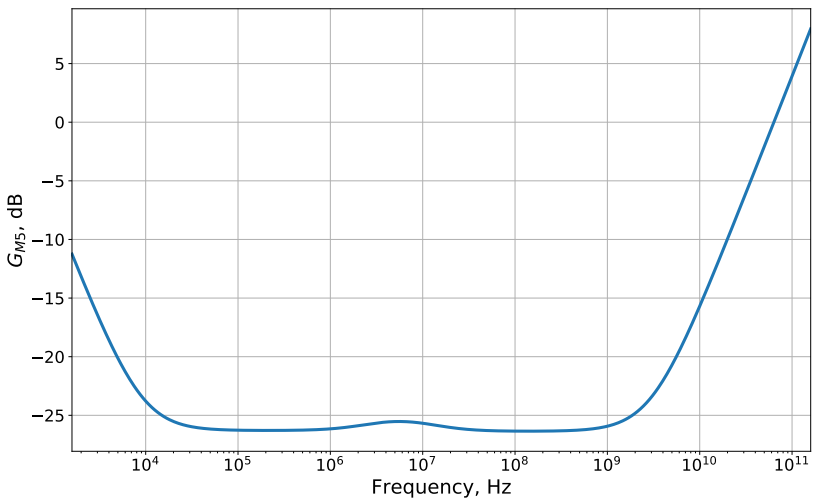

Fig. 2.23. Shaping filter due to G_{M5}

Fig. 2.24 shows the performance of our complete noise model for a set of model gains. Similarly to the case of the flicker noise on M_1, here the parameter $K_\mathrm{f}/\left(C_\mathrm{ox}WL\right)$ for M_5 shall be also computed based on the transistor geometry and is equal to 10 nA for the base gain.

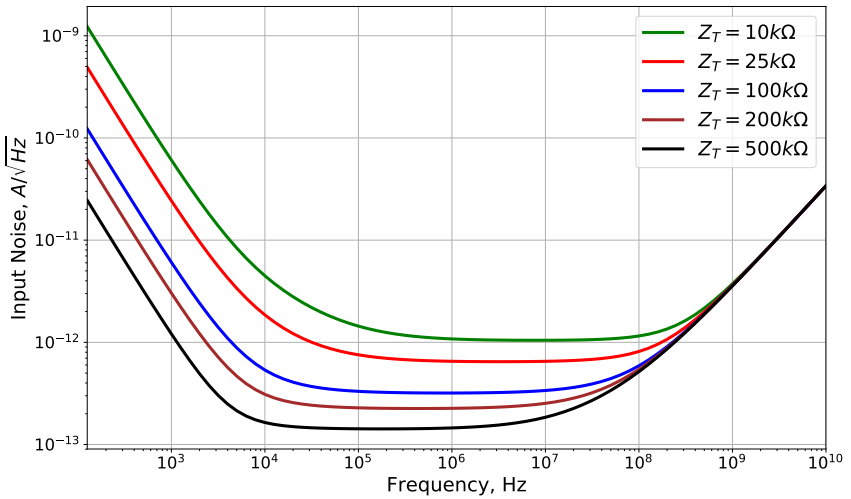

Fig. 2.24. Analytically calculated complete input-referred noise performance for programmable-gain configuration

Apart from the low-frequency M_5 noise, the non-ideal behavior of a practical biasing circuit is also often neglected by other authors while deriving the noise models. Exactly this was suggested in (Keshri, 2010), where the author kept the noise component due to R_2 while assuming perfect biasing circuit with no additional source of noise (e.g. when the voltage headroom allows implementation of low-noise transistor-based biasing). However, for a realistic circuit operating under voltage headroom constraint with resistive biasing such a model would clearly result in an over-optimistic estimation for the noise level in mid-range frequencies. Note that none of the components of resistive noise was considered in the series of works of Shahdoost (see the latest work (Shahdoost et al., 2016)). While biasing noise was similarly ignored due to transistor-based implementation and assumption of effectively infinite resistance, the noise from R_2 was neglected due to its presumably minor impact. According to the author, the noise contribution was solely due to the noise of the core amplifier (our first noise component $\overline{i^2_{\mathrm{nt}'}}$ presented above).

The assumption on perfect biasing for M_1 results in yet another difference with the models so far presented in the literature. Authors typically assumed a pure reactive input impedance (see the series of works of Shahdoost and work

(Ghanad & Dehollain, 2016)), resulting in:

$$\overline{i^2_{\mathrm{n,TIA}}} \approx \overline{v^2_{\mathrm{n,OpAmp}}} \left[C_{\mathrm{T}} + \frac{C_1}{1 + C_1/C_2} \right]^2 s^2. \tag{2.66}$$

Technically, the model can be derived from our noise model when one assumes perfect biasing $R_{\mathrm{bias},1} \to \infty$. Then the model for the input impedance becomes:

$$\lim_{R_{\mathrm{bias},1} \to \infty} Z_{\mathrm{in}} = \frac{1}{1 + s\left(C_{\mathrm{T}} + \frac{C_1 C_2}{C_1 + C_2}\right)} \approx \frac{1}{1 + s\left(C_{\mathrm{T}} + C_2\right)} \approx \frac{1}{1 + sC_{\mathrm{T}}}. \tag{2.67}$$

As we can see, in the capacitive network, the input impedance is formed by C_{T} in parallel with the series connection of C_1 and C_2. Since the C_{T} dominates the input impedance, we can re-arrange the noise model above and since for capacitive feedback holds TIA $C_1 \gg C_2$, we obtain:

$$\begin{aligned} \overline{i^2_{\mathrm{n,TIA}}} &\approx \overline{v^2_{\mathrm{n,OpAmp}}} \left[C_{\mathrm{T}} + \frac{C_1 C_2}{C_1 + C_2} \right]^2 s^2 \\ &\approx \overline{v^2_{\mathrm{n,OpAmp}}} \left[C_{\mathrm{T}} + \frac{C_1 C_2}{C_1} \right]^2 s^2 = \overline{v^2_{\mathrm{n,OpAmp}}} \left[C_{\mathrm{T}} + C_2 \right]^2 s^2, \end{aligned} \tag{2.68}$$

and the latter expression is yet another simplified noise model as reported by (Keshri, 2010).

How already known noise models from literature compare with the noise model developed by us can be seen in Fig. 2.25, where the performance of noise model from the literature is shown for our set of circuit parameters (the model from the series of works of Shahdoost is even simpler as it ignores the noise component from R_2 as well). The major differences include the absence of both flicker noise components (from M_1 and M_5) as well as the absence of the noise due to $R_{\mathrm{bias},1}$. The latter is consistent with the discussion above, since the biasing circuit has generally been assumed to have infinite resistance in the literature. Finally, the noise model assumes constant TIA gain in form of $R_2\,(1 + C_1/C_2)$ when scaling the noise from R_2. However, as we have demonstrated above, the real circuit has a distinct pass-band behaviour, and a significant low-frequency component, due to the shaping nature of the inverted Z_{T}, is ignored when mapping the R_2 noise. As we can see, the noise models that are commonly found in the literature are inadequate for estimating the noise level in realistic capacitive feedback TIAs when voltage headroom constraints are applied and such models may underestimate the noise level in all frequency ranges.

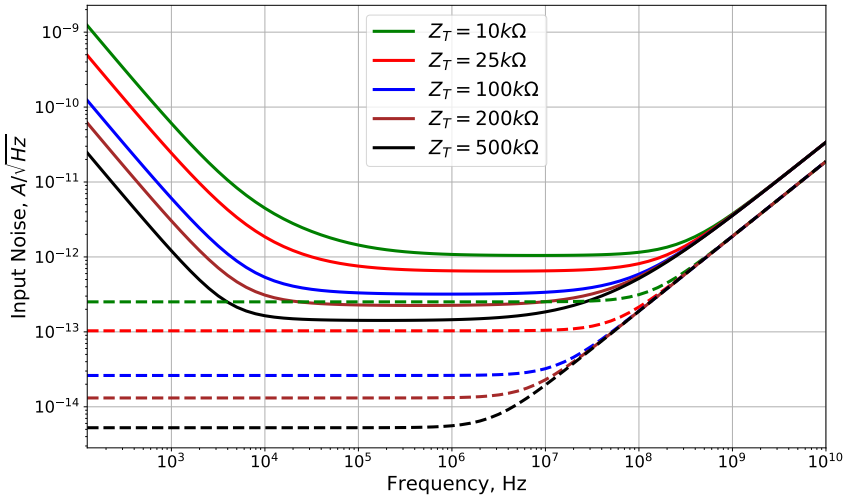

Fig. 2.25. Noise model from Keshri applied for our set of circuit parameters (dashed lines) and our developed complete noise model for the same set of parameters (solid lines)

One can notice here a distinct advantage of the proposed TIA architecture when compared to the classical resistive feedback approach suggested for OTDR design in series of works of Charlamov. In simple resistive feedback TIA both the dominating noise source and the gain are mainly defined by the feedback resistor R_{F}. However, in the proposed design the baseline noise is defined by a set of different parameters along with a more complex gain definition. We believe that exactly this feature of the proposed architecture provides a better trade-off of the main TIA parameters when compared to the classical design. While in classical resistive approach almost everything depends on a single value of R_{F}, in capacitive feedback the dependency is far more complex which provides the designer far more tuning knobs for design optimization and tuning.

2.8. Cascode in Current Source

A careful inspection of the gain for the exemplary model shown in Fig. 2.4 reveals that the gain adjustment method based on two tuning knobs ($R_{\mathrm{bias},1}$ and C_1) may be also a weakness of the proposed design. For the exemplary realistic CMOS configuration presented above the pass-band in the middle is not sufficiently flat, as the gain in the low-frequency range is mainly adjusted with the bias resistor of M_1, while C_1 dominates for higher frequencies. In the particular example above this leads to a drop of around 0.7 dBΩ and this may have a negative impact on the

performance of the OTDR front-end. The small pitch or step appears in the middle and it cannot be easily tuned out by a careful selection of both tuning parameters available to the user. In practice, this means that the pitch is likely to be maintained no matter how we choose our two tuning knobs, and how flat it is depends on correspondence between both values, as well as the rest of the circuit parameters. This may make the process of the gain adjustment far less intuitive.

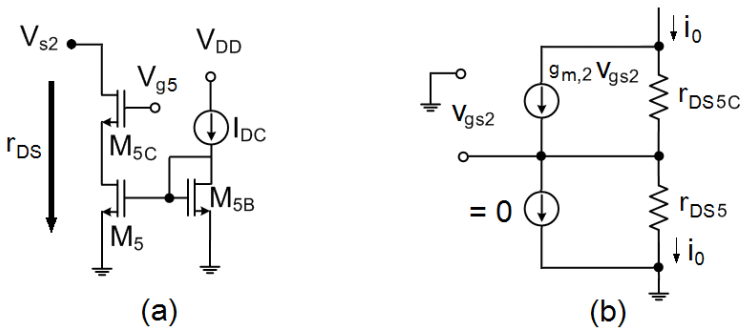

Fig. 2.26. Proposed cascode implementation of the current source (a) and small-signal equivalent circuit for design calculations (b)

The remedy to the problem comes from the observation that the exact position of the transition point between $R_{\mathrm{bias},1}$ and C_1 dominated frequency ranges depends on the value of $r_{\mathrm{DS}5}$. In practice, by making the value of $r_{\mathrm{DS}5}$ larger we shift this transition point to lower frequencies. This means that by greatly increasing $r_{\mathrm{DS}5}$ we may improve the flatness and enlarge the gain plateau defined by C_1/C_2 gain, while reducing or even completely eliminating the frequency range controlled by $R_{\mathrm{bias},1}$. In practice, a significant increase of $r_{\mathrm{DS}5}$ can be achieved using a cascode circuit with the transistor $M_{5\mathrm{C}}$ on the top of M_5 as shown in the Fig. 2.26 (a). This design change affects our proposed amplifier in several ways. First, as intended, it allows us to achieve much larger values of $r_{\mathrm{DS}5}$ when compared to the older design based solely on M_5. Furthermore, much larger $r_{\mathrm{DS}5}$ makes the adjustment of $R_{\mathrm{bias},1}$ mostly unnecessary, since the frequency range controlled by this parameter is largely or even completely eliminated. Here, a single albeit relative large value of $R_{\mathrm{bias},1}$ (in order of several hundreds of kΩ), may suffice for all the gain configurations. This increase in $R_{\mathrm{bias},1}$ itself results in a significant drop in the noise current $\overline{i^2_{\mathrm{nr}1}}$ which plays the determining role for the noise level exactly in the operating range of frequencies (our gain plateau). Even though the mathematical model for Z_{T} itself remains the same, it can be now parametrized differently with effective $r_{\mathrm{DS}5}$ up to hundreds of kΩ or even in MΩ range. As a result, the programmable gain can be now tuned only by the adjustment of C_1 and the circuit for variable $R_{\mathrm{bias},1}$ is not necessary. This in itself makes the circuit simpler and

further reduces the chip footprint. A drawback of this approach is that $R_{\mathrm{bias},1}$ is now large and shall be implemented in an area-efficient method (for example, as an NMOS circuit similar to other $R_{\mathrm{bias},1}$ values in our previously described design shown in Fig. 2.14).

As for the model, we will replace the previously used r_{DS5} with r_{DS} and consider a small-signal AC model as shown in Fig. 2.26 (b), where for the effective AC impedance of M_5 and $M_{5\mathrm{C}}$ we can derive:

$$\begin{aligned} r_{\mathrm{DS}} &= \frac{v_{\mathrm{DS}}}{i_{\mathrm{DS}}} = \frac{i_0 r_{\mathrm{DS5}} + (i_0 - g_{\mathrm{m},2} \cdot v_{\mathrm{gs2}})\, r_{\mathrm{DS5C}}}{i_0} \\ &= \frac{i_0 r_{\mathrm{DS5}} + (i_0 + g_{\mathrm{m},2} \cdot r_{\mathrm{DS5}} \cdot i_0) \cdot r_{\mathrm{DS5C}}}{i_0} \\ &= r_{\mathrm{DS5}} + r_{\mathrm{DS5C}} + g_{\mathrm{m},2} \cdot r_{\mathrm{DS5}} \cdot r_{\mathrm{DS5C}} \\ &\approx g_{\mathrm{m},2} \cdot r_{\mathrm{DS5}} \cdot r_{\mathrm{DS5C}}, \end{aligned} \tag{2.69}$$

where:

$$v_{\mathrm{gs2}} = -r_{\mathrm{DS5}} i_0. \tag{2.70}$$

Clearly, the mechanism allows us to reach much larger effective values of r_{DS} using an area-efficient cascode current source and to obtain a flat frequency response with just a single C_1 tuning knob. A minor disadvantage of the proposed scheme is that the design needs a larger voltage drop over M_5 when compared to the older design without cascode.

2.9. Discussion

In the sections above we have developed a model for an area-efficient implementation of the capacitive feedback CMOS TIA operating under the voltage headroom constraints. We have selected a classical implementation of the core voltage amplifier and proposed a concept for a programmable-gain version using a simultaneous adjustment of two circuit parameters. An advantage of the suggested approach is that we have been able to solve the voltage headroom problem while staying with a single-stage approach. This allows the design to benefit from the noiseless feedback feature of the reference capacitive feedback architecture. The programmable-gain approach is extremely simple and at the same time allows an independent adjustment of the low- and high-frequency behavior. An improvement is also suggested using an additional cascode transistor for the current source formed by M_5 which allows to reach the target bandwidth while ensuring flat passband.

For comparison of the noise sources let us recall that in SFB TIA for sufficiently large gain A the transimpedance gain becomes equal to R_{F}. Thus, for the

given set of transimpedance gains, one could compute the noise current due to the feedback resistor as:

$$\frac{\overline{i^2_{\mathrm{nr,SFB}}}}{\Delta f} = \frac{4\mathrm{k_B}T}{R_\mathrm{F}}. \tag{2.71}$$

Then at room temperature and R_T = 10 kΩ the noise current becomes around 1.3 pA/$\sqrt{\mathrm{Hz}}$ and correspondingly smaller noise currents down to 0.18 pA/$\sqrt{\mathrm{Hz}}$ for the configuration with the largest gain of R_T = 500 kΩ. When compared to our design, the noise floor of SFB TIA due to feedback resistor is 27% worse (1.3 pA/$\sqrt{\mathrm{Hz}}$ vs. 1.01 pA/$\sqrt{\mathrm{Hz}}$) for the smallest gain configuration with R_T = 10 kΩ and the difference increases to 50% for the largest gain R_T = 500 kΩ , where the noise floor of the capacitive feedback TIA becomes around 0.12 pA/$\sqrt{\mathrm{Hz}}$ when compared to 0.18 pA/$\sqrt{\mathrm{Hz}}$ for the classical resistive feedback. Of course, this simplistic analysis does not consider the additional noise generated within the core operational amplifier. Though the noise level of the classical configuration is from 27% to 50% worse than that of the proposed design under the rest of conditions being identical, the difference is not that significant and one may argue that the noise levels are within the reach of the classical design as well. Here, however, one may recall that for classical SFB TIA one gets the bandwidth as:

$$BW_{-3\mathrm{dB}} = \frac{A+1}{2\pi R_\mathrm{F} C_\mathrm{T}}. \tag{2.72}$$

For simplicity we can consider a simple single stage CS core voltage amplifier as in our case with $A \approx g_{\mathrm{m},1} R_1$ as we are likely to use similar architecture for the core voltage amplifier to overcome the supply headroom constraints. For some selected circuit parameters (e.g. we take those from Chapter 3) we end up in A equal to 28 (recall that $A = G_1$). The substitution of this moderate gain to the expression above leads us to the bandwidth of below 660 MHz and this value is fairly far from the required 1 GHz. On the other hand, for the given core amplifier the bandwidth of 1 GHz can be achieved for the gain $R_\mathrm{F} \approx$ 6.6 kΩ , which almost factor 1.5 less than the required gain. Thus, with this we clearly see that even though similar noise floors are, in principle, within the reach of classical SFB TIA designs, a simple single-stage CS-based design would not be able to reach the required noise-bandwidth combination. At the same time, our proposed architecture provides almost 1.5x better trade-offs when compared to reference architecture typically used for OTDR applications (see (Charlamov, 2013) for the further details). Clearly, the performance in terms of the noise is even better if we use our suggested design with cascode current source.

Further modifications are also possible. For example, an interesting idea was tossed in (Ghanad & Dehollain, 2016), where the buffer stage formed by R_2 and M_2 was replaced with a push-pull buffer. The approach does not require R_2 as

the current through C_1 is directly sensed by a low impedance stage such as the current mode mixer. Apart from several advantages such as larger voltage swings, smaller amplifier input impedance, the push-pull buffer stage increases the capacitive loading of the voltage amplifier which is undesirable for higher speed applications. Note that the work addressed the design of the TIA for magnetic resonance imaging with operation frequencies below 150 MHz where this design may be still acceptable.

The capacitive feedback topology as presented in this work was originally proposed as a solution to the problem of the most important noise contribution in the bandwidth of the amplifier caused by the feedback resistor R_{F} in classical SFB TIA. However, the described approach is not the only one, and an alternative configuration with capacitive feedback exists as shown in Fig. 2.27 (Ferrari et al., 2007; Rajabzadeh et al., 2018). Here the idea is to introduce a completely reactive element C_1 to replace the original R_{F}. Even though the capacitor does not contribute to the noise, it is still desirable to have the transimpedance gain which is constant over the required bandwidth. This requires the introduction of another stage to keep the overall transimpedance gain constant. The overall gain of such system within the desired signal bandwidth becomes:

$$Z_{\mathrm{T}} = -\frac{1}{j\omega C_1}\left(-j\omega C_2 R_{\mathrm{F}}\right) = \frac{C_2}{C_1} R_{\mathrm{F}}. \tag{2.73}$$

When compared to the classical resistive feedback model of the same gain, this integrator-differentiator topology improves the bandwidth of the system due to pole-zero cancellation. At the same time, the gain expression demonstrates the same advantage as our suggested capacitive feedback design, where a large ratio of two capacitors supports the realization of a large transimpedance without using area-inefficient feedback resistor R_{F}. The design also has the benefit of reducing the thermal noise of the resistor by factor C_2/C_1. However, the increase in system bandwidth is only maintained when the poles introduced by the actual frequency response of the core amplifiers occur at frequencies higher than those corresponding to the pole introduced by the capacitance in parallel to R_{F}. Although this is believed to be often the case when dealing with gains higher than 100 MΩ, a detailed analysis of the frequency response of the system with respect to the poles of the core amplifiers may be needed (Keshri, 2010). On the other hand, the design may result in the bandwidth practically approaching the gain-bandwidth product of the core amplifier. The design, when compared to SFB TIA, also provides more degrees of freedom to choose the overall gain against noise and speed.

One of the major disadvantages of this alternative topology is that the feedback capacitance C_1 of the integrator stage must be discharged to prevent its saturation due to the input leakage current. Obviously, a simple additional feedback resis-

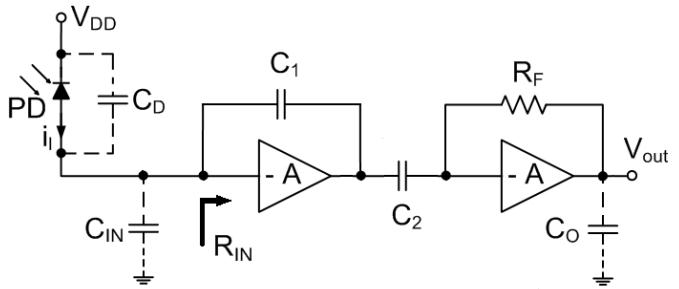

Fig. 2.27. Basic configuration of integrator-differentiator TIA with capacitive feedback

tor in parallel with C_1 cannot be used as a large value is required to minimize the noise (Ferrari et al., 2007). An alternative solution is to place a MOSFET switch in parallel with the integrator capacitance, which discharges it when the output voltage reaches a defined threshold. Unfortunately, this simple switch sets a limit measurement time available which may make the integration impossible as the reset may happen too often. In (Ferrari et al., 2007) the authors proposed an alternative solution composed of the feedback with a continuous reset circuit (leaky integrator). Although the noise includes an additional term due to the shot noise of the spill transistor in the reset circuit, the authors demonstrated that the overall noise can be kept relatively small. Still, for the equal transimpedance gain of both topologies (our proposed capacitive feedback and alternative integrator-differentiator), the input-referred noise contribution of the former is lower as compared to integrator-differentiator (Keshri, 2010). Finally, caused by the more complex design and large overhead of the reset circuit, the power consumption of the integrator-differentiator TIA is higher when compared to capacitive feedback TIA of otherwise equivalent performance. An interesting drawback of this design is the frequency-dependent dynamic range when using a feedback filter (Rajabzadeh et al., 2018). Thus, the integrator-differentiator approach from above does not have any advantages with respect to the given OTDR requirements when compared to our proposed conceptually simpler capacitive feedback TIA.

Another interesting extension was suggested in (Wilson & Chen, 2014), where a low-power switched capacitor integrating TIA was designed for bio-sensing applications. The authors suggested this topology as a remedy for a problem of capacitive feedback TIA requiring high-impedance biasing circuits. However, we have demonstrated that circuit-level solutions can be used to address the problem of high-impedance circuits. Moreover, the usability of the switched capacitor integrating TIA for applications above several hundreds of MHz is questionable. Note that originally the authors in (Wilson & Chen, 2014) demonstrated low noise and high gain for the system with a cut-off frequency of around 10 MHz which is far

below the OTDR requirement of 1 GHz. In general, such designs may require special considerations for effects due to charge injection and may need dedicated switch noise minimization or cancellation measures for high sensitivity applications (Wilson, 2014).

2.10. Conclusions of Chapter 2

Research results presented in Chapter 2 address dissertation problem No. 1, raised in Chapter 1 conclusions section. Chapter 2 can be summarized with the following concluding statements:

1. An original TIA architecture with arrays of discrete-controlled feedback capacitors and resistances in the biasing circuit has been proposed to implement programmable-controlled gain, wide bandwidth and low noise.
2. Due to ever-improving CMOS technological nodes and decreasing supply voltages, the problem of the voltage headroom in the development of support bias circuits is becoming especially important. Therefore, this TIA architecture offers an original PMOS transistor-based biasing circuit for the source follower which allows to replace the fully resistive circuit and thus reduce the area occupied by the chip. The value of the biasing voltage can be controlled by changing the geometry of the involved transistors.
3. An accurate mathematical model for the transimpedance gain has been developed and evaluated. The model allows to identify and calculate the parameters of the major components of the suggested design and improves the overall modeling accuracy in the frequency range up to 1 GHz.
4. The main sources of noise present in the proposed TIA architecture were studied and their impact on the total noise current spectral density was evaluated. Analytic expressions for the respective noise components have been provided along with noise minimization suggestions. A generalized mathematical model of the noise current spectral density was developed, on the basis of which a detailed study of the TIA architecture and verification of the suggested model was performed. Further noise improvement was suggested by integrating a cascode into the current source within the source follower block.

3

Design and Investigation of Capacitive Feedback TIA

In this chapter, the experimental results (analytical modeling and numerical simulation) are presented. Based on the design methodology described in Chapter 2, fixed-gain and programmable-gain circuits have been evaluated with respect to the specification requirements for OTDR applications. First, classical TIA performance measures such as gain and bandwidth have been evaluated including the sensitivity of the performance to the variation of the total input capacitance. Later, the noise performance of the developed circuits was investigated. Finally, the preliminary results for gain and noise for the alternative configuration with cascode current source in the source follower circuit are shown and impact of the temperature on the noise performance for cascode version is discussed. The results presented in the chapter confirm the target performance of the amplifier to be achieved using relatively simple CS-based single-stage core voltage amplifier with source follower. The results also support the claim on the suitability of the architecture to serve as the basis for robust programmable-gain TIA configuration with respect to all gain configuration requirements up to gain of 500 kΩ. The simulation also confirms the power dissipation of the proposed design to be within the requirement being below 50 mW and a significant margin for the power budget is still available for further modifications and improvements.

Several versions of fixed-gain realizations and a programmable-gain versions were implemented in 0.18 μm 1.8 V CMOS and 0.25 μm 2.5 V BiCMOS. The base

TIA configuration had demonstrated the target 80 dBΩ transimpedance gain and bandwidth around 1.0 GHz with the noise level below 2.0 pA/$\sqrt{\text{Hz}}$ when implemented in 0.18 µm CMOS and 80 dBΩ transimpedance gain and bandwidth around 0.9 GHz with the noise level around 1.6 pA/$\sqrt{\text{Hz}}$ when implemented in 0.25 µm BiCMOS. Several versions with programmable-gain were designed for five gain configurations (10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ). The programmable-gain configuration occupies the area of only 150 µm × 160 µm with power consumption of 21 mW for all gain configurations when implemented in 0.18 µm CMOS and 200 µm × 180 µm with power consumption around 29 mW when implemented in 0.25 µm BiCMOS.

The research results, presented in this chapter, have been already partially demonstrated at the international "eStream" (Romanova & Barzdenas, 2020b) scientific conference as well as published in (Romanova & Barzdenas, 2021a) paper.

3.1. Processes and Tools Analysis

CMOS is the IC fabrication process which employs complementary and symmetrical pairs of both p-type and n-type MOSFET transistors (PMOS and NMOS device pair). Although the technology is mostly famous for constructing complex digital logic circuits such as processors, memory chips etc., it had been also successfully employed for designing analog circuits including image sensors, RF circuits and different types of integrated transceivers for numerous communication systems.

As we have already mentioned in Chapter 1, classical CMOS has a number of advantages which made it the technology of choice for the most of modern consumer electronics. From production point of view, the technology offers higher packaging density, low manufacturing costs per device and high yield along with ability to integrate almost arbitrary complex functions in a single chip. A CMOS transistor is also an almost ideal switching device with extremely low static power dissipation. Typically, devices in CMOS possess also a number of extremely useful features such as high noise margins, scalable threshold voltages and so-called bi-directional capabilities, because drain and source of the transistor are interchangeable. Unfortunately, there is no free lunch and there are also certain limitations related to CMOS devices. Among those one can mention typically lower transconductance, lower capabilities for output drive current (may have implications while driving higher capacitive loads). Finally, typically the circuits in CMOS have high input impedance and low drive current along with higher delay sensitivity to load which may limit the fan out capabilities. Still, the perspectives of CMOS for design of highly integrated optical receivers have been recognized already several decades ago with a good overview on the peculiarities of using it for optical communication systems described in (Razavi, 2002).

For our proposed design we use a commercially available 0.18 µm CMOS from TSMC (0.18 µm CMOS Logic or MS/RF, General purpose 1.8 V/3.3 V) with the key specification shown in Table 3.1. Although as a technology being relatively old, TSMC claims to be the first one in the world to offer this technological node as early as 1998. At the moment this can be considered as a well-proven and mature process well supported by an extensive IP ecosystem. At the same time it is an affordable technology with good RF capabilities which also makes it an excellent choice for educational applications and low-cost solutions. The technology supports from 3 to 6 metal layers, STI, triple well, RI poly resistor and ultra-thick metal.

On the other hand, the bipolar technology provides a number of advantages over standard CMOS. In spite of higher power dissipation, lower packing density and lower swing logic, the bipolar technology offers much higher switching and I/O speeds, lower input impedance (high drive current) and higher transconductance. Moreover, the technology also offers higher current drive per unit area and higher gain and, at least in general, better noise performance along with improved high frequency characteristics. Compared to CMOS, the bipolar technology also offers improved capabilities for analog circuits and lower delay sensitivity to load. Finally, it offers high unity gain bandwidth at lower currents and, differently from CMOS, bipolar devices are unidirectional.

The BiCMOS technology combines both the Bipolar and CMOS technology in a single IC. While using this process one can benefit both from the low power dissipation, large noise margins and greater packing densities of CMOS as well as from faster switching speed and large current capabilities of bipolar technology. For the BiCMOS-based design we use the CMOS part of the 0.25 µm SiGe:C BiCMOS technology from IHP Microelectronics: a German R&D institution with a focus on development of advanced wireless and broadband communication systems. The institute is located in Frankfurt/Oder and runs an 8 inch pilot line for research and low volume prototyping. The cross-section of five metal layer 0.25 µm SiGe:C BiCMOS and the corresponding cross-section of a real MOSFET in 0.25 µm SiGe:C BiCMOS technology are shown in Fig. 3.1 (a) and Fig. 3.1 (b) correspondingly.

The chosen technology provides integrated HBTs with cut-off frequencies up to 500 GHz including complementary devices and is mostly employed for products in fiber optics, payload in space, wireless communication, radar design and THz imaging. For the proposed design we have selected an established SG25H3 technology. This is a 0.25 µm technology with a set of npn-HBTs ranging from higher RF performance ($f_{\mathrm{T}}/f_{\mathrm{max}}$ = 110/180 GHz) to higher breakdown voltages up to 7 V. Cadence-based mixed signal Design Kit is available for this technology which makes the design relatively straightforward. The CMOS section of the key specifications for SG25H3 BiCMOS from IHP Microelectronics is shown in

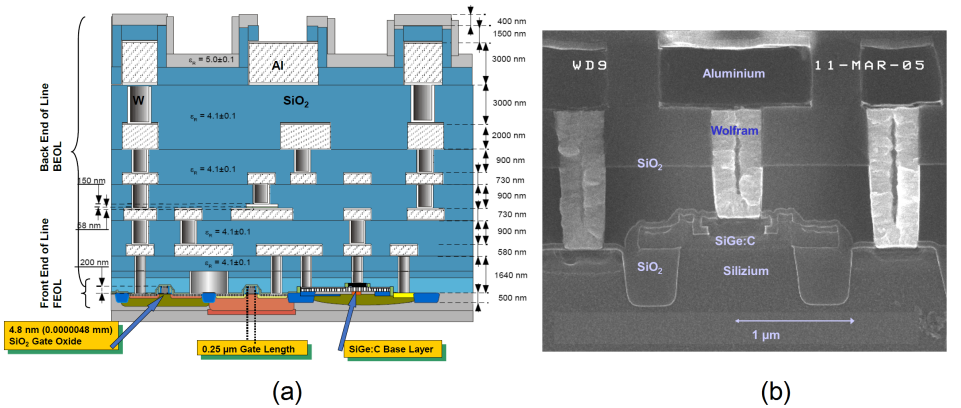

Fig. 3.1. Cross-section of 5 metal layer 0.25 µm SiGe:C BiCMOS technology (a) and cross-section of a MOS transistor in 0.25 µm SiGe:C BiCMOS technology (b) (courtesy of IHP Microelectronics).

Table 3.1. The major part of the work presented here was done using Virtuoso platform tools from Cadence Design Systems, Inc. Virtuoso platform forms a set of commercial tools for professional development of full-custom ICs and includes the development of the schematic entry, behavioral modeling, circuit simulation, custom layout, physical verification, extraction and back annotation functionality. As a full commercial tool (university licensed for this work) it allows a standalone design of arbitrarily complex circuits up to physical representation level (i.e. circuit design composed to the level of transistors, resistors, etc.), modeling and layout design.

Table 3.1. Key specifications of BiCMOS from TSMC and SG25H3 BiCMOS from IHP Microelectronics (CMOS section)

Feature	Value in TSMC CMOS	Value in IHP BiCMOS
Technology node (µm)	0.18	0.25
CMOS core supply (V)	1.8	2.5
C_{MIM} (fF/µm^2)	1.0-2.0	1.0
Poly Res (Ω/□)	313	210-280
NMOS V_{th} (V)	0.5	0.6
PMOS V_{th} (V)	−0.51	−0.6

For the design and implementation of the proposed capacitive feedback TIA Cadence Virtuoso Platform version IC6.1.6 was used. For the CMOS technology the design kit TSMC T018CMSP018K3 was employed, while for the BiCMOS technology the IHP Microelectronics (Frankfurt (Oder), Germany) the design kit

SG25H3_617_rev1.7 was used. In both cases the specifications of the technologies have been analyzed for their general suitability for the target TIA design (e.g. f_{T}, etc.). When the suitability of the technologies is confirmed, one starts with the schematic entry and the general circuit design as detailed in Chapter 2 of the presented work. When the schematic entry is finished, errors are checked using the design rules check (DRC) to ensure that the circuit is compliant with the design rules. Circuit-level simulation using vendor-supplied models, is performed to ensure that the design as a whole conforms to specification. When the general behavior of the circuit and its compliance to the requirements is confirmed, one starts with the topological entries for separate elements and later proceeds to complete layout following vendor's design rules and specifications while considering analog layouting issues described in details in subsequent section. Analysis and correction of the geometrical errors is performed in order to get a final circuit layout. Finally, the performance of the layout is compared against circuit-level simulation and corresponding corrections are implemented if necessary. The final step typically confirms that acceptable IC performance deterioration is observed in post-layout simulation when compared to the results expected on schematics level. Although typically this step results only in layout correction with the basic schematics remaining intact, in some challenging cases of high-performance analog design it may be also necessary to revisit the solution on schematics level or even introduce changes to some of the requirements.

3.2. Layout Design

Based on the design methodology described in the previous chapter, the proposed amplifiers were implemented and optimized using TSMC 0.18 µm CMOS process and the corresponding CMOS part of the IHP 0.25 µm BiCMOS. The basic configuration of the fixed-gain capacitive feedback TIA is shown in Fig. 3.2. (a). At the beginning both the biasing voltages V_{in} and V_{g2} were implemented using a pure resistive biasing circuit similar to the one shown in Fig. 3.2. (b). However, further analysis of V_{g2} biasing voltage had demonstrated that the footprint minimum under given voltage headroom constraints can be achieved using PMOS-based circuit as shown in Fig. 3.2. (c). In order to implement the concept of programmable-gain TIA, the ratio of capacitances C_1 and C_2 was changed by keeping C_2 constant and C_1 changing in G_{ADJ}<1:4> steps as depicted in Fig. 3.2. (d), while the biasing voltage circuit V_{in} was modified so that EN<1:4> would connect the transistors $M_{\mathrm{n1}}...M_{\mathrm{n4}}$ in series, thus effectively changing the value bias resistance $R_{\mathrm{bias,1}}$ (see Fig. 3.2. (e)).

In the most general case, as some block diagram is usually the first step in the design procedure, the floor-planning is usually the first step in the layout process.

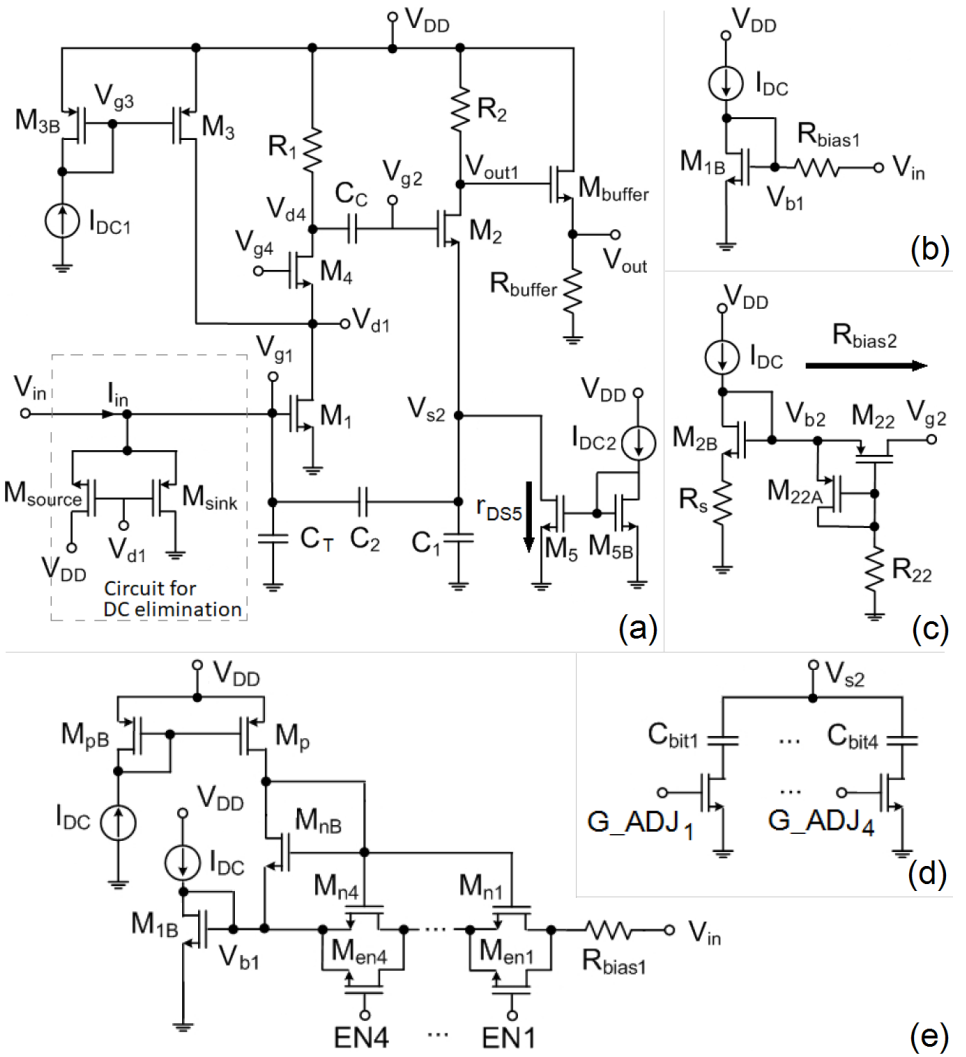

Fig. 3.2. Proposed capacitive feedback TIA: (a) fixed-gain capacitive feedback TIA; (b) resistive biasing circuit; (c) PMOS-based biasing circuit; (d) implementation of C_1 switch for programmable-gain; (e) mixed resistive/NMOS-based programmable-gain implementation for $R_{\mathrm{bias},1}$

After taking care of the all customer pin-out requirements or corresponding packaging restrictions, the designer has some freedom in positioning the blocks and components. This is often done quite close to the block diagram. However, there are some common-sense rules which have to be taken into considerations:

- Place power components and sensitive functional blocks as far apart as

possible in order to minimize the substrate noise, coupling and thermal gradients.

- Do not place sensitive functional blocks in chip corners (stress gradients).
- Try to arrange components and blocks according to their functional context and their supply.
- Place components with high matching requirements as close together as possible.
- Minimize the length of sensitive signal paths.
- Minimize the length of noisy signal or power paths.
- Try to place power supply and related return pins as close as possible.

Some of the above recommendations shall also apply, and are especially relevant while refining the layout, but the foundation shall be already built in the floor-planning phase. Even though our TIA as a circuit is far from complex industrial ASICs, we have tried to follow all the best practices above to ensure a minimum degradation of the circuit performance.

There are several special issues to be considered when one wants to implement a high-performance analog circuit. Also a simple model states that the chip substrate is considered as “ground”, due to the substrate’s limited conductivity, capacitive coupling through the substrate, injection and collection of carriers this assumption may lead to certain unwanted effects. For example, any substrate contact at the wafer surface, that is connected to a voltage that is different from the "deep substrate" potential, will cause some turbulence in the surface potential around it. This variation in local surface potential can in turn modulate the threshold voltages and disturb sensitive analog circuits.

It may be also important to mention several issues which shall be considered when aiming for a higher performance design. One of those is a so-called well-proximity-effect. This is one of the layout-dependent effects which is caused by dopant ions that are scattered of the photoresist side walls into the areas close to the well edges. A MOS transistor (affects both NMOS and PMOS) close to a well edge will therefore have different device parameters than a transistor far away from a well edge. The effect becomes more critical the smaller the CMOS process gets. As we target relatively conservative 0.18 µm process, this issue is not so prominent, but shall be nevertheless considered when one opts for a higher performance design. As a rule of thumb, the problem can be mitigated by having a transistor gate more than 3 µm distance from the edge of the well.

Another effect to consider is the STI stress effect. This is yet another type of the layout-dependent-effects and mostly affects smaller CMOS processes, where the isolation between active devices is achieved by implanting STI regions between the devices. These STI regions create unintentional compressive mechanical stress

in the active areas of the MOSFET devices. Finally, if MOSFETs are placed with merged active areas, the effect of the induced stress is bigger for the outer devices compared to the inner devices of the group. The problem is solved by trying to place the transistors with a spacing to each other so that their active areas do not merge. If this is not possible, the stress effect can be reduced by placing enough dummy devices at the ends of the shared active region.

Another issue is due to layout pattern-dependent variation in the inter-level dielectric thickness. To improve the yield and minimize the impact on the circuit performance one shall fill the layout globally and uniformly with metal or dummy metal. For example, DRC rules exist which check that the global metal density is larger than 30% for every metal layer. Similar to other effects, its importance increases the smaller the CMOS process becomes.

Table 3.2. Parameters for programmable-gain TIA with difference implementations (see Fig. 3.2 for details of the circuit)

Parameter	Units	CMOS w/o cascode	BiCMOS w/o cascode
R_1	[Ω]	350	400
R_2	[Ω]	500	400
C_2	[pF]	0.11	0.055
$g_{\mathrm{m},1}$	[S]	0.08	0.09
$g_{\mathrm{m},2}$	[S]	0.0028	0.002
C_{T}	[pF]	0.7	0.7
C_{C}	[pF]	6.0	6.0
$R_{\mathrm{bias},2}$	[MΩ]	4.0	3.0
r_{DS5}	[kΩ]	23.0	22.0
$C_1 @ Z_{\mathrm{T}} = 10$ kΩ	[pF]	2.4	2.0
$R_{\mathrm{bias},1} @ Z_{\mathrm{T}} = 10$ kΩ	[kΩ]	17.0	17.0
$C_1 @ Z_{\mathrm{T}} = 25$ kΩ	[pF]	6.0	5.0
$R_{\mathrm{bias},1} @ Z_{\mathrm{T}} = 25$ kΩ	[kΩ]	42.5	42.5
$C_1 @ Z_{\mathrm{T}} = 100$ kΩ	[pF]	24.0	20.0
$R_{\mathrm{bias},1} @ Z_{\mathrm{T}} = 100$ kΩ	[kΩ]	170.0	170.0
$C_1 @ Z_{\mathrm{T}} = 200$ kΩ	[pF]	48.0	40.0
$R_{\mathrm{bias},1} @ Z_{\mathrm{T}} = 200$ kΩ	[kΩ]	340.0	340.0
$C_1 @ Z_{\mathrm{T}} = 500$ kΩ	[pF]	120.0	100.0
$R_{\mathrm{bias},1} @ Z_{\mathrm{T}} = 500$ kΩ	[kΩ]	850.0	850.0

The final set of the design values for the most important circuit parameters including the values for the adjustable parameters C_1 and $R_{\mathrm{bias},1}$ for selected gain-bandwidth configurations is shown in Table 3.2. Note that we do not explicitly list transistor dimensions as they are technology specific and can be easily calculated from circuit design parameters. Most of the values are coming from design process outlined in Chapter 2 under the requirements to achieve a particular gain and

bandwidth as well due to limitation for the circuit to operate from 1.8 V power supply for CMOS or 2.5 V supply for BiCMOS. Still, several decisions on the parameter choice can be outlined. For example, the value of R_1 is selected so that the current of several mA shall flow. This allows us to achieve the required V_{d4} voltage at the output of the core amplifier. The design also requires R_2 to be close to R_1 in order to provide enough current for the source follower transistor M_2. A practical design also requires $g_{\mathrm{m},2}$ to be from 10 to 30 times smaller than the $g_{\mathrm{m},1}$. Note that differently from $g_{\mathrm{m},1}$, the transconductance of the source follower has minor effect on the overall gain, but has a tremendous effect on the bandwidth and therefore can be effectively used as a bandwidth tuning knob when the gain plateau is achieved. The value of $R_{\mathrm{bias},2}$ defines the high-pass behavior and lower cut-off frequency and shall be selected in combination with r_{DS5} in order to obtain the required low-frequency behavior of the circuit. The key circuit parameters C_1, C_2, $R_{\mathrm{bias},1}$ and r_{DS5} define the gain at the mid-frequency plateau. In the case of non-cascode implementation, $R_{\mathrm{bias},1}$ is mostly responsible for the low-frequency part, while the value of C_1 controls the higher frequency part. However, as we elaborated in Chapter 2, in cascode-based implementations the value of $R_{\mathrm{bias},1}$ is set to constant, but relatively large value, while only C_1 is adjusted for the the required gain. On the other hand, while in non-cascode implementation the value of r_{DS5}, typically in the range of tens of kΩ, for cascode implementation the value shall be set to a relatively large value in the range of several hundreds kΩ. As we discussed before, the capacitance C_2 can be selected just several times the smallest value realizable with the given technology so that the feedback network C_1/C_2 has the smallest possible footprint.

As was explained before, the values of $R_{\mathrm{bias},1}$ and C_1 shall be interpreted as cumulative ones for both the resistance and capacitance for the non-cascode implementations, while in cascode implementation this is necessary only for C_1. Clearly, the configurations with the largest gains (R_{T} = 200 kΩ and 500 kΩ) are the most demanding in terms of the consumed area with the cumulative capacitance reaching 120 pF for C_1. The adjustable $R_{\mathrm{bias},1}$ (for non-cascode cases) is implemented as a resistor only for the configuration with the smallest gain R_{T} = 10 kΩ, while for the rest transistor-based implementations with equivalent resistivity are adopted to save the chip area. Although only one resistance is required to implement the cascode, its value is quite large (correspondingly 2 MΩ or 0.48 MΩ), and here also a transistor-based implementation is necessary. The results shown in Table 3.2 confirm that the proposed methodology (see Chapter 2 for details) for the design of programmable-gain TIA in CMOS is extremely simple, because the values for $R_{\mathrm{bias},1}$ and C_1 simply linearly scale up with the required gain. While the base gain of R_{T} = 10 kΩ can be configured with C_1 and $R_{\mathrm{bias},1}$ set to initial values, the next gain configurations are obtained by simply up-scaling the base values of these one/two tuning knobs with the required gain factor. The power dissipation

of all configurations is nearly constant and is around 21 mW for CMOS design and 29 mW for BiCMOS design while running correspondingly from 1.8 V and 2.5 V power supplies. Note also that neither of the proposed programmable gain configurations is a constant-bandwidth design. Therefore, with the given base TIA there is a clear limit on the maximum achievable gain.

As we have demonstrated in the previous chapter, a PMOS-based formulation of the biasing circuit allows an area-efficient implementation of the circuit where the chip die area is actually limited by the capacitor C_1 for the configuration with the largest gain. Interestingly, the authors in (Wilson, 2014; Wilson & Chen, 2014), while looking for topologies for low-noise and high-gain bio-sensing applications, have eliminated our proposed architecture from the candidate list. Their argument was exactly due to the area penalty of high impedance biasing circuit which consumes large amount of die area. As we see, this argument renders itself invalid with proper modification of the biasing circuits as we have demonstrated in Chapter 2. With the design above we confirm that the reference capacitive feedback topology, due to its inherent advantages, shall be kept while only the biasing circuit has to be replaced with an area-efficient configuration.

3.2.1. Results in CMOS

Fig. 3.3 shows the layout of the initial 10 kΩ fixed-gain capacitive feedback TIA with pure resistive biasing for both M_1 and M_2 (see (a), underlying design is as shown in Fig. 2.2 with both resistive biasing circuits shown in Fig. 2.3), the layout of the 10 kΩ fixed-gain implementation with optimized PMOS-based biasing circuit for M_2 (see (b), underlying design is as shown in Fig. 2.2 with resistive biasing circuit shown in Fig. 2.3 (a) for M_1 and PMOS transistor-based biasing circuit shown in Fig. 2.12 (b) for M_2) and the corresponding final programmable-gain version with five gain configurations (10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ) in (c) (design as is in (b) with $R_{\mathrm{bias},1}$ and C_1 switch arrays implemented as shown in Fig. 2.14 and Fig. 2.15). The original solution with a pure resistive biasing for both M_1 and M_2 occupies 200 µm × 130 µm (excluding contact pads) due to MΩ resistance in the second bias circuit. The transistor-based solution for M_2 reduces the TIA area down to 130 µm × 70 µm (excluding contact pads) with an area reduction of around 65% compared to the base design. Finally, the programmable-gain configuration, which is the main goal of our research, covers an area of 150 µm × 160 µm, which is 2.6 times the area compared to the fixed-gain solution with PMOS-based biasing for M_2, but still smaller than our first fixed-gain configuration with pure resistive biasing. Here the implementation of C_1 for larger gains consumes around 50% of the design area and is, therefore, mainly responsible for the area increase in the programmable-gain configuration. In the case higher gain is needed or in order to minimize the footprint of the design, the C_1 capacitors

which correspond to the largest R_{T} values (200 kΩ and 500 kΩ or larger) may be implemented as off-chip components, e.g. using discrete ceramic capacitors. Additionally, the programmable-gain version with cascode I_{SS} was implemented in TSMC CMOS. The design is a bit simpler as no gain adjustment mechanism for $R_{\mathrm{bias},1}$ is needed, but due to its larger value a transistor-based implementation was used. This improved design with single adjustment parameter occupies similar area as the non-cascode counterpart and is not shown here.

The design area is comparable to a previously reported (Charlamov & Navickas, 2015) programmable-gain amplifier for OTDR applications based on resistive feedback in 0.35 µm CMOS. However, in the proposed design we have achieved significantly better performance for all TIA configurations with almost no penalty in the die area.

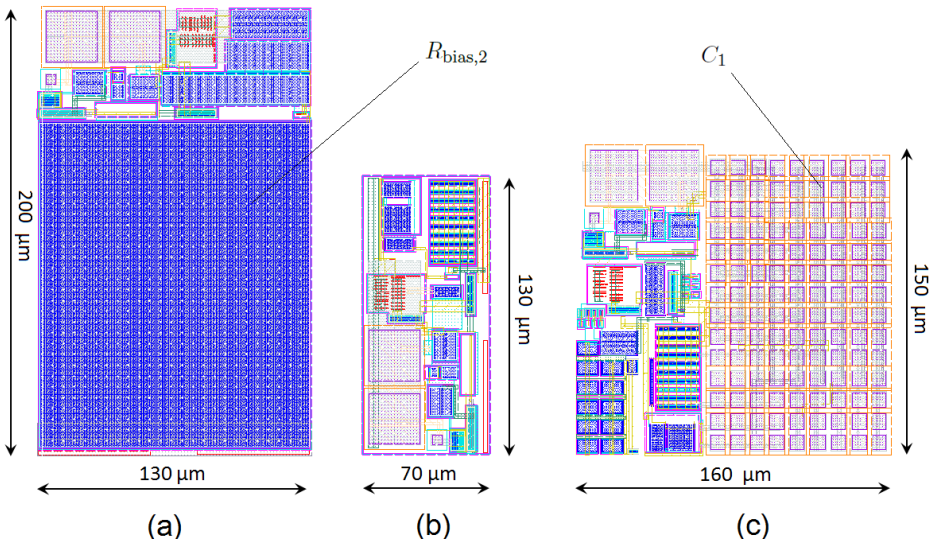

Fig. 3.3. Layout of the implemented TIA using TSMC 0.18 µm CMOS process: (a) fixed-gain 10 kΩ capacitive feedback TIA with pure resistive biasing; (b) fixed-gain 10 kΩ capacitive feedback TIA with PMOS-based biasing for M_2; (c) corresponding programmable-gain implementation of capacitive feedback TIA for five gain-bandwidth configurations

3.2.2. Results in BiCMOS

As we discussed above, the same design concepts were also evaluated and tested using 0.25 µm BiCMOS technology (using CMOS part) from IHP Microelectronics. Here only the programmable-gain versions (with and without cascode I_{SS}

and both with PMOS-based M_2 biasing) were implemented with the design shown in Fig. 3.4 for the non-cascode BiCMOS implementation. The design occupies 200 µm × 180 µm area and is 50% larger than the equivalent non-cascode I_{SS} implementation in TSMC 0.18 µm CMOS discussed above. Similarly to the case of CMOS, a version with cascode I_{SS} was also implemented and evaluated for the set of target gains. This improved design with single adjustment parameter occupies similar area as the non-cascode version and is not shown here.

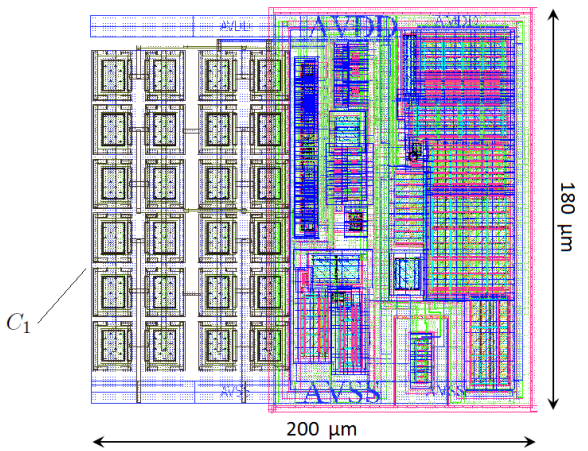

Fig. 3.4. Layout of the implemented programmable-gain capacitive feedback TIA with non-cascode I_{SS} for five gain-bandwidth configurations using IHP 0.25 µm BiCMOS process

3.3. Gain Analysis

First, let us start from the performance analysis in terms of the gain for our proposed programmable-gain configurations. Fig. 3.5 shows the results of the post-layout simulation against the analytical model developed in Chapter 2 for all five gain-bandwidth configurations in TSMC CMOS. First, we clearly see the importance of properly covering the low-frequency behavior of the practical circuit, which has been ignored by the simpler models known so far in the literature. Regarding the results of the Cadence simulation and the analytical model, even though the low- and mid-frequency behavior is fairly well covered, some discrepancy can still be seen for the high-frequency range (above the upper cut-off frequency). Comparison of the obtained results with the data in Fig. 2.4 also confirms that this mismatch is common for both models. However, we consider that it isn't very important, since the mismatch affects the frequencies far above the band-

width of interest. For all configurations the Cadence simulation shows pretty good match with the gain discrepancy below 5% in terms of dBΩ for the bandwidth of interest below 1 GHz. The only structural discrepancy is the mismatch between the simulation and analytical model in the transition point between two regions in the pass-band. Interestingly, the Cadence simulation provides a rather flat pass-band while the model still predicts a small pitch. This, however, can be explained by the fact that the analytical model still does not take into account all the parasitics, and significant efforts were spent in fine tuning of the design and implementation. In all gain configurations a small pitch or bending in the point connecting the low-frequency region in the pass-band can be seen, where the region with $R_{\mathrm{bias},1}$ control of the gain meets the region with the gain control mostly affected by C_1. In general, we see that the derived analytical model provides a very good fit to the simulation and confirms the proposed concept of the programmable-gain TIA, since all the configurations are able to reach their target values in terms of the gain. While the base configuration with R_{T} = 10 kΩ reaches the target bandwidth of 1 GHz, the versions with larger gains demonstrate a corresponding shrinking of the bandwidth going down to 0.03 GHz for the gain configuration with Z_{T} = 500 kΩ. As we already explained in Chapter 2, this is actually an expected result as we did not try to target the equal-bandwidth design. Even more, there are reasons to believe that the bandwidth of 1 GHz is close to the limit for the provided generic capacitive feedback architecture for the gain of 10 kΩ and, clearly, larger gains are hardly possible without reduction in the bandwidth. Note that we do not provide the discrepancy between the simulation data and the model of Shahdoost. As we have demonstrated in Chapter 2, the model proposed by Shahdoost is a simple first-order approximation of the real circuit and is based on numerous simplifications not valid for real circuit developed under voltage headroom constraints. Moreover, the model ignores the pass-band behavior of a real circuit and, therefore, the model results in qualitatively different behavior for low-frequency range.

Fig. 3.6 shows the results for the same design implemented and tuned IHP 0.25 µm BiCMOS process. Note that due to different supply voltages (1.8 V CMOS vs. 2.5 V BiCMOS) and technology details the set of parameters to be used here is slightly different when compared to the TSMC CMOS design discussed above. In general, our previous discussion on TSMC-based design fully applies here including the pass-band separation to two regions, model mismatch for the very high frequencies and reduction in the achievable bandwidth from 0.9 GHz to approximately 0.03 GHz for the gain configuration with Z_{T} = 500 kΩ. Note that we have been able to obtain even better matching between the analytical model and the Cadence results when compared to the CMOS-based implementation with the discrepancy below 3% for the bandwidth of interest. The results confirm that the linear C_1 and $R_{\mathrm{bias},1}$ parameter scaling model suggested in Chapter 2 is still valid, while a better match when compared to CMOS may be also a tuning or

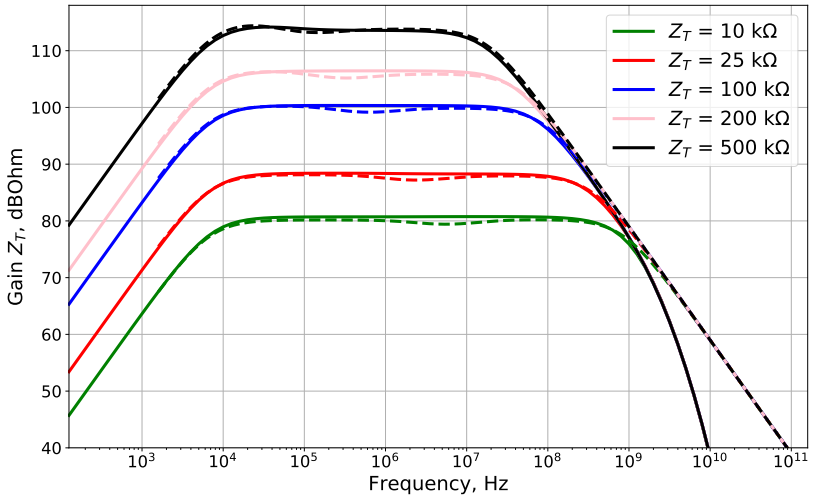

Fig. 3.5. Proposed analytical model Z_{T} and Cadence simulated transimpedance gain for programmable-gain TIA configuration in TSMC 0.18 µm CMOS. Solid lines are due to simulation, dashed lines are due to developed gain model

parametrization coincidence. The slightly better match can also be partly explained by the fact that BiCMOS uses a 2.5 V power supply, and voltage headroom problems can be more easily avoided. The only fundamental difference, when compared to our previously discussed design using CMOS, is that we were not able to reach the target bandwidth of 1 GHz and the maximum attainable value was around 0.9 GHz. This indirectly confirms that the required base TIA specification in terms of the gain-bandwidth product is likely to be beyond the capabilities of this relatively old technology and there is a necessity to use the more advanced technology nodes.

The derivation of the model in Chapter 2, as well as all the results presented above, are provided while ignoring the trivial modeling of the output buffer. The results of the Cadence simulation for the transimpedance gain correspondingly before and after the output buffer for all five gain-bandwidth configurations in TSMC CMOS (version without cascode in I_{SS}) are shown in Fig. 3.7. As expected, the buffer results in a consistent and predictable gain drop of around 3 dB for all gain configurations. This amplifier is a typical building block, therefore the behavior is similar for other configurations and those results are not shown here.

As it was already mentioned, the envisioned usage of TIA in OTDR application implies a set of additional requirements on the amplifier's performance which are often ignored for CMOS TIA designed for pure high-speed data transmission applications. One of these requirements is phase linearity, because the numerous techniques which are often used for bandwidth extension, such as inductive peak-

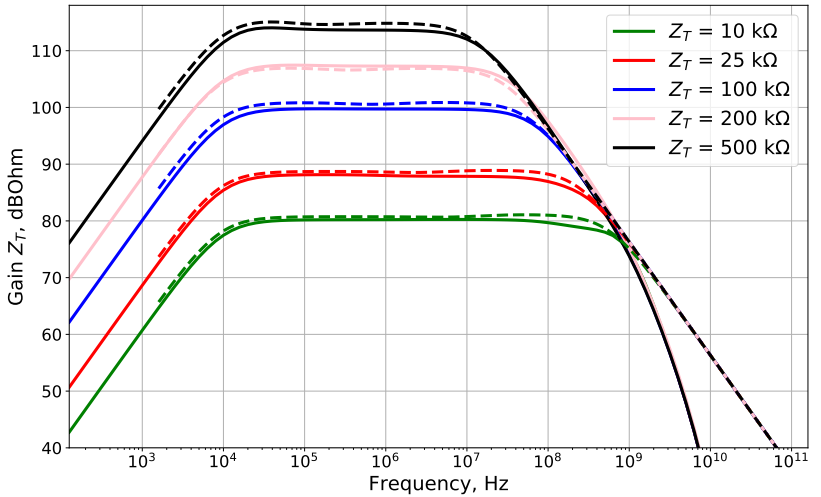

Fig. 3.6. Proposed analytical model Z_{T} and Cadence simulated transimpedance gain for programmable-gain TIA configuration in IHP 0.25 µm BiCMOS. Solid lines are due to simulation, dashed lines are due to developed gain model

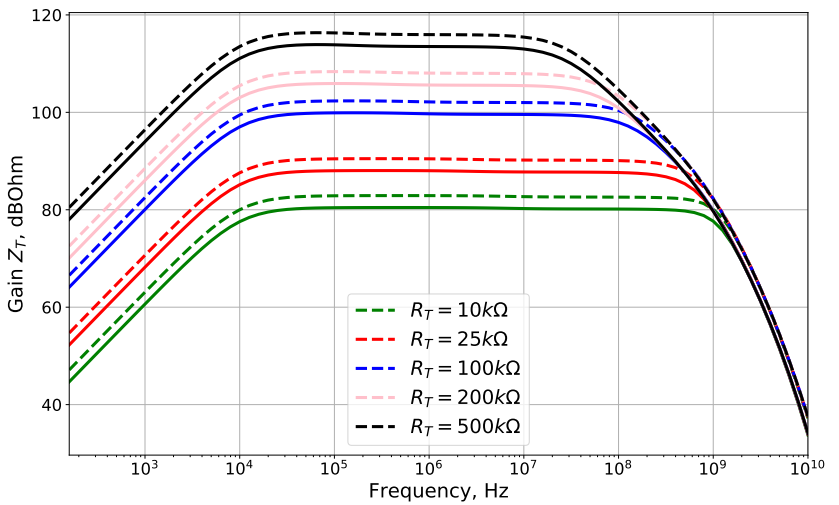

Fig. 3.7. Cadence simulated transimpedance of programmable-gain TIA configuration in TSMC 0.18 µm CMOS with and without output buffer. Dashed lines before the output buffer, solid line are for the gain after the output buffer

ing, result in a trade-off between the bandwidth enhancement and the linearity of the phase. Similarly, classical methods of the bandwidth enhancement also result in an increase of the group delay variation and therefore it is important to have a look at the phase performance of the developed circuit. An example of the Cadence

simulated phase performance for programmable-gain TIA configuration in TSMC 0.18 µm CMOS with non-cascode I_{SS} is shown in Fig. 3.8, where for comparison the phase model as proposed by Shahdoost is plotted as a dashed line. Obviously there is a fundamental difference between the phase of the real circuits and the first-order low-pass approximation proposed by Shahdoost. First, while the simplified models start from the zero degrees phase at DC, the actual circuits show non-trivial behavior with the first segment representing the low-frequency stop-band of the TIA. Further mismatch to a simple first-order approximation can be found at higher frequencies, where a simple approximation converges to a trivial $-\pi/2$ phase shift.

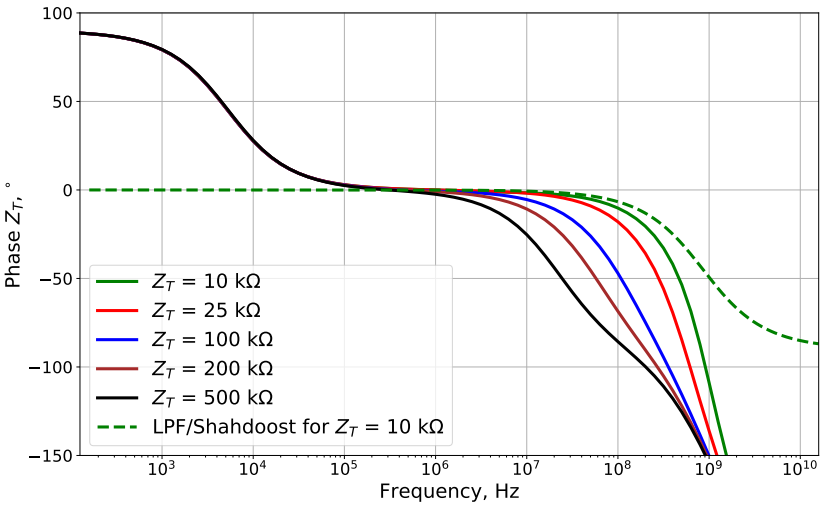

Fig. 3.8. Cadence simulated phase of Z_{T} for programmable-gain TIA configuration in TSMC 0.18 µm CMOS with non-cascode I_{SS}. Solid lines are the results of the Cadence simulation, while the dashed line is the first-order approximation proposed by Shahdoost and computed for R_{T} of 10 kΩ

With regard to the phase performance of our proposed model, a comparison between the analytical solution and the post-layout simulation for the programmable-gain configuration in 0.18 µm CMOS can be seen in Fig. 3.9. Here we observe a fairly good fit of both results up to rather high frequencies where our model, similarly to the model of Shahdoost, converges to a trivial $-\pi/2$ phase shift. Obviously, this is related to the unmodeled slope in the gain for very high frequencies as seen, for example, in Fig. 3.5. Note that this slope mismatch in the transimpedance gain is also common for our and previously known models, but is of a lesser importance as it takes places beyond the bandwidth of interest.

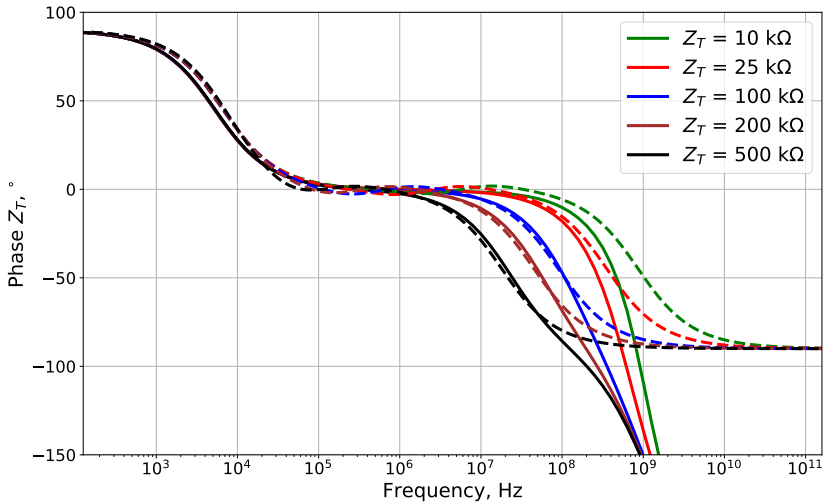

Fig. 3.9. Proposed analytical model Z_{T} and Cadence simulated transimpedance phase for programmable-gain TIA configuration in TSMC 0.18 µm CMOS. Solid lines are due to simulation, dashed lines are due to developed phase model

Finally, we can use the post-layout simulation to check the dependency of the gain on the actual C_{T} when the circuit was designed and tuned for a different C_{T} value. Fig. 3.10 shows the transimpedance gain of the CMOS non-cascode I_{SS} implementation for R_{T} = 10 kΩ with the design targeting 0.7 pF, while different C_{T} is effectively present at the input. As expected, the difference is mainly visible in the high-frequency where the gain is defined by ratio of the feedback capacitors C_1/C_2, while the low-frequency region of the plateau controlled by $R_{\mathrm{bias},1}$ remains unaffected. As predicted by the theory, smaller C_{T} results in an increased bandwidth, while gain increase or decrease step in the plateau becomes visible depending on whether the actual C_{T} is larger or smaller than the target value.

3.4. Time-Domain Analysis

The behavior of the developed amplifier in time-domain can be visualized using the eye-diagrams. Although the technique is typically used to confirm the performance of TIAs developed for data transmission application, we can also employ the technique to assess quality of the eye opening. An example of such diagram for the R_{T} = 10 kΩ configuration in CMOS with PRBS frequency of 100 MHz (usage existing "PRBS" module in Cadence) and the input pulse 10 µA peak-to-peak is shown in Fig. 3.11. Similar performance can be seen for other gains and programmable-gain implementations for both used technologies.

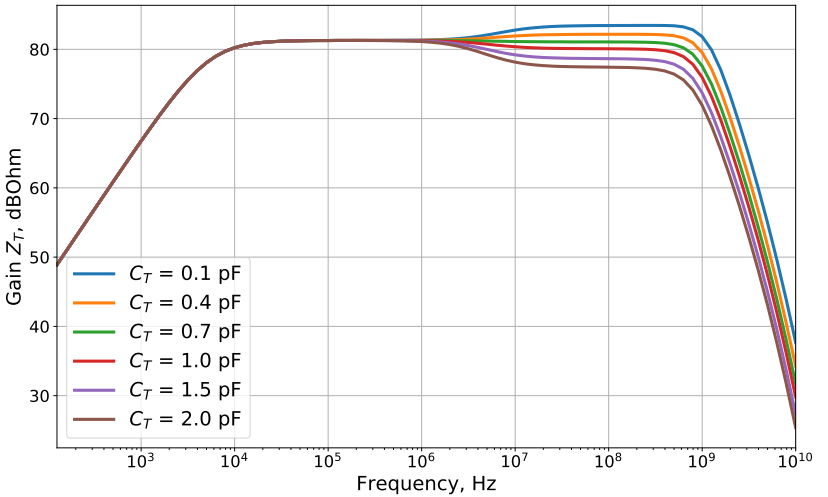

Fig. 3.10. Cadence simulated sensitivity of the transimpedance gain to the actual value of C_{T}, when TIA designed for the reference value of C_{T} = 0.7 pF. Results shown for programmable-gain TIA configuration in TSMC 0.18 µm CMOS

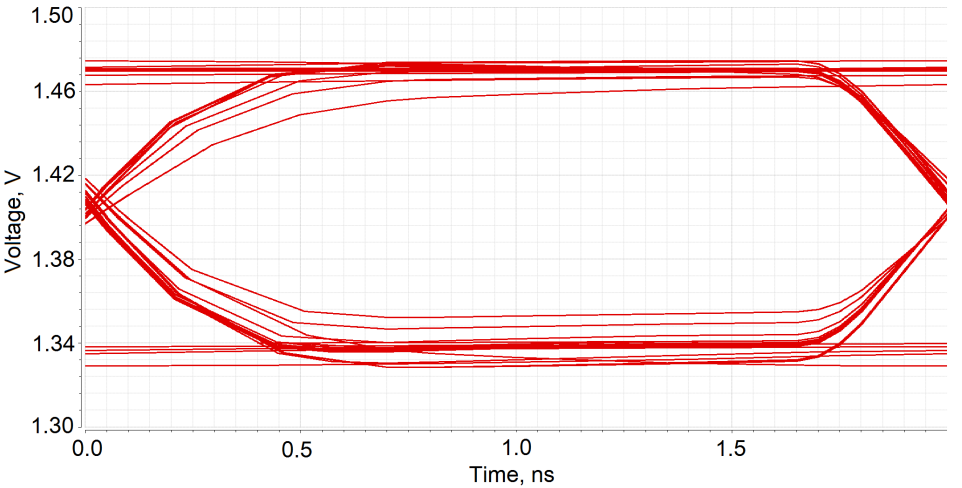

Fig. 3.11. Eye-diagram for R_{T} = 10 kΩ configuration using PRBS with pulse duration of 2 ns

3.5. Noise Analysis

Similarly to the case of the gain, we will start the noise analysis by considering the programmable-gain TIA configurations without cascode I_{SS} when implemented

in TSMC 0.18 µm CMOS (see Fig. 3.12) and using IHP 0.25 µm BiCMOS (see Fig. 3.13). In the case of CMOS, rather good fit can be seen for low- and high-frequency ranges as well as the fit in the noise minimum point with the mismatch below 10% at the frequency of 500 MHz for the 10 kΩ configuration and similar performance for the minimum points at other gains. A slight mismatch between the developed noise model can be seen in the transition from low- to mid-frequency ranges, where the post-layout simulated noise somehow exceeds the prediction of the model. While the same is true for the BiCMOS-based implementation, it is also better suited to the problematic segment from low- to mid- frequency range. Mismatch below 15% at the frequency of 500 MHz for the 10 kΩ configuration can be seen caused by the offset the analytical prediction and the simulation. Additionally to the effects discussed before, we also clearly see the famous $1/f$ behavior of the M_1 flicker noise in the low-frequency region. This effect (due to square-root dependency in PSD) gives the 10 dB/decade drop. However, this drop is mainly responsible for the noise behavior between 10 kHz and 1 MHz, while for very low frequencies we observe the noise with slope around 20 dB/decade which cannot be explained by the flicker noise M_1 and was a reason to include the impact of M_5 flicker noise into the model as well.

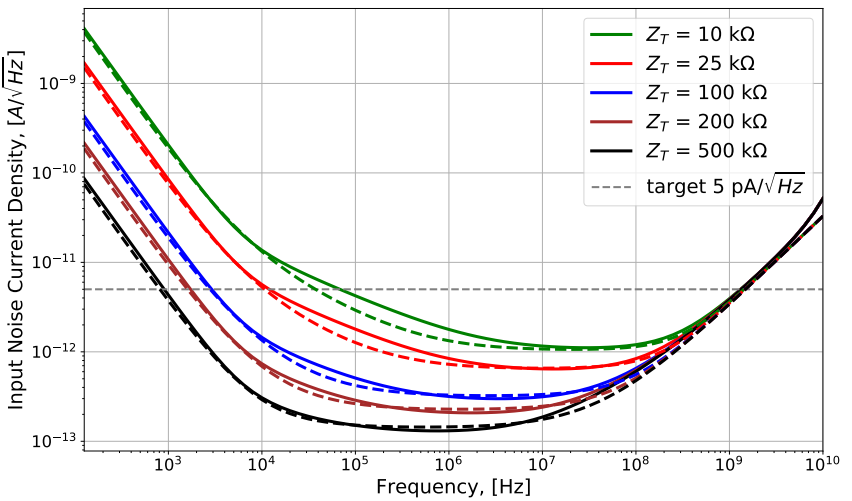

Fig. 3.12. Proposed analytical model for the input-referred noise current density and Cadence simulated noise for programmable-gain TIA configuration in TSMC CMOS. Solid lines are due to simulation, dashed lines are due to developed combined model

Although both configurations result in similar minimum noise points (noise minimum point mismatch below 15%), the design based on BiCMOS seems to

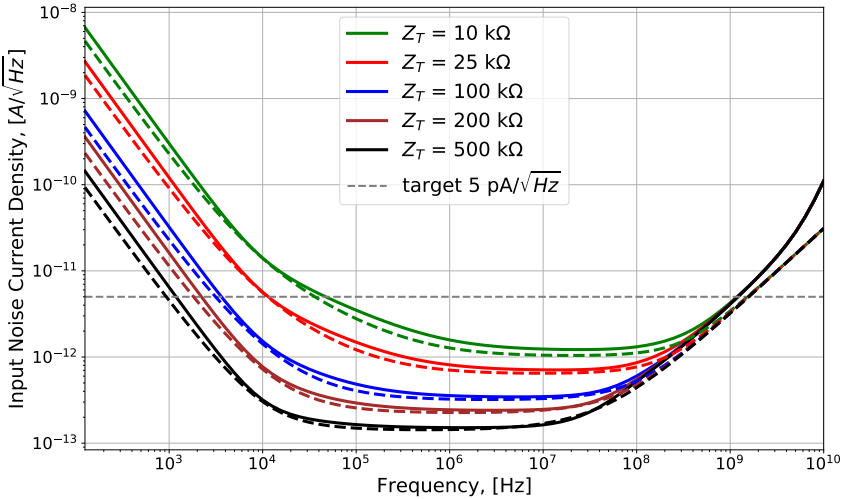

Fig. 3.13. Proposed analytical model for the input-referred noise current density and Cadence simulated noise for programmable-gain TIA configuration in IHP BiCMOS. Solid lines are due to simulation, dashed lines are due to developed combined model

have a wider plateau with constant minimum noise. This means that the BiCMOS design allows the designer to reach minimum noise for a wider set of operating frequencies when compared to that of our CMOS. One of possible explanations for the mismatch is that BiCMOS is an older technological node and, correspondingly, larger transistors shall be used. Even though we were not able to reach the target bandwidth of 1 GHz using this BiCMOS (0.9 GHz had been achieved for target gain of 80 dBΩ), the noise performance is apparently better over wider frequency range when compared to more modern but noisier low-cost 0.18 µm CMOS.

Here, similarly to the case of the gain, we do not try to provide numerical discrepancy values for the noise model of Keshri or Shahdoost. As we have demonstrated in Chapter 2, those models strongly underestimate the real noise floor of the developed circuit and ignore three out of five major noise components. Thus, these models show qualitatively different behavior from that observed for the real circuit, so that any analysis of discrepancies is rather misleading.

3.6. Corner Analysis and Monte Carlo Simulation

In practice we are often interested in the robustness of the suggested design against global process variation. The robustness is typically confirmed by performing a corner analysis and Monte Carlo simulation for the most important parameters of

the circuit. When implementing Monte Carlo statistical analysis, the sampling for the transistor, resistor and capacitor parameters is done from the associated normal distributions (Gaussian). Within the modeling step 200 samples are taken for each relevant component and the distributions of the main parameters of the circuit are analyzed. Note that the same is done for the corner analysis. There one starts by considering three configurations: typical-typical ('tt', standard), slow-slow ('ss', the worst) and fast-fast ('ff', the best) cases. Each of these cases corresponds to the corner case for characteristics of transistors or other elements derived from statistical parametric models of the manufacturing process intended to be used. With the help of this modeling we can observe the maximum deviation for the most relevant circuit parameters, i.e. the spread from the worst configuration to the best one. By estimating this spread with 3σ confidence one is able to ensure that the obtained parameters (i.e. gain of the amplifier) of the produced integrated circuits will be within this range. This spread is affected both by the circuit architecture itself, circuit-level design decisions and the quality of the layout and, therefore, shall be performed once the integrated solution is ready for production. In the

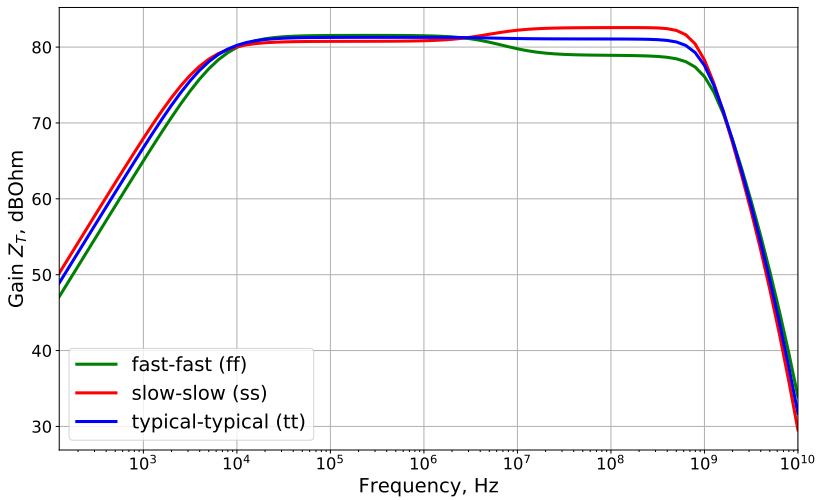

Fig. 3.14. Corner analysis for the transimpedance gain in the case of TSMC 0.18 µm CMOS implementation and Z_{T} = 10 kΩ configuration

case of transistors, fast and slow corners correspond to the values of the carrier mobilities that are higher and lower than the normal (typical) values. Additionally to the transistors, the used corner libraries have implemented 8% variation in resistances and 15% variation in capacitance is taken (correspondingly decrease in percentage for 'ff' configuration and increase for 'ss' configuration). The results are presented for the case of TSMC 0.18 µm CMOS implementation. For simplic-

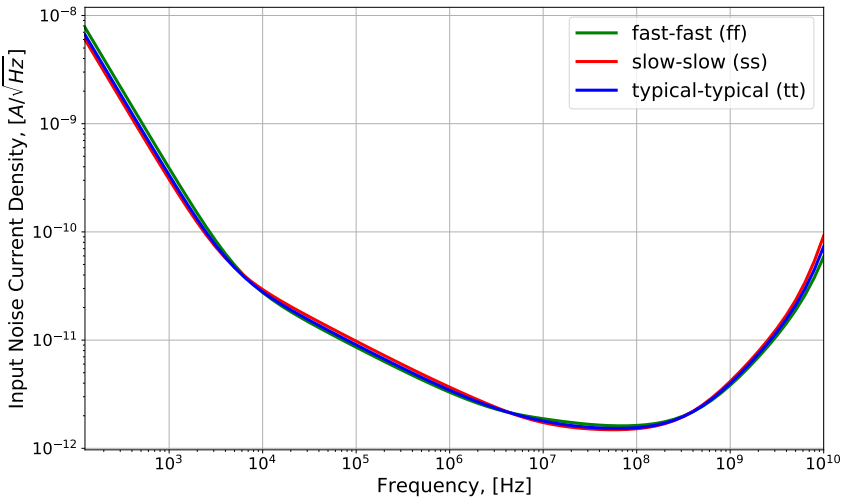

Fig. 3.15. Corner analysis for the noise current density in the case of TSMC 0.18 µm CMOS implementation and Z_{T} = 10 kΩ configuration

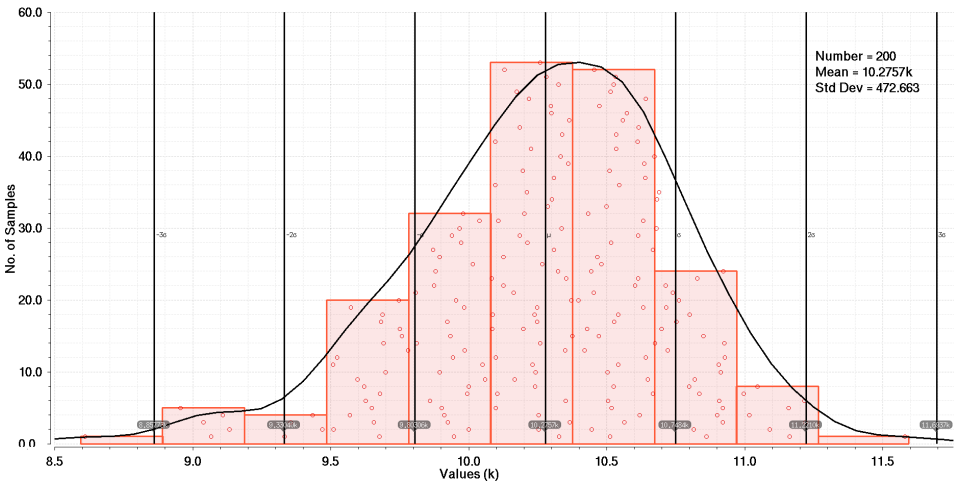

Fig. 3.16. Histogram of the transimpedance gain from Monte Carlo simulation in the case of TSMC 0.18 µm CMOS implementation and Z_{T} = 10 kΩ configuration. Sample size is 200 and computed mean gain 10.2757 kΩ with standard deviation 472 Ω (measurements performed at 100 MHz)

ity, we demonstrate here only the results for the base configuration with gain Z_{T} = 10 kΩ, as for other gains the results are similar. Fig. 3.14 shows the result for the transimpedance gain, where Fig. 3.15 shows the results for the input-referred noise current spectral density.

As already discussed in Chapter 2, the gain plateau contains two regions, and not surprisingly, changing the process also affects gain differently in both regions for lower and higher frequencies. The obtained gain behavior is consistent with the analysis on C_1 impact presented in Chapter 2. For the gain parameter plot, the value of C_1 essentially controls the level of the high-frequency region, while the low-frequency region, mainly controlled by $R_{\mathrm{bias},1}$, shows reduced dependence on parameter variation. With regard to the noise performance, only minimal dependency of the noise on variation of circuit parameters can be observed in Fig. 3.15.

Fig. 3.16 shows the results of the Monte-Carlo simulation for the transimpedance gain in the case of TSMC 0.18 µm CMOS implementation and the base gain configuration with Z_{T} = 10 kΩ. For the sample size of 200 the mean gain is 10.27 kΩ with standard deviation of approximately 472 Ω when measured at the frequency of 100 MHz. Note that the standard deviation is below 5% of the nominal gain (around 4.6%). In terms of dBΩ, 1-σ deviation is around 0.4 dBΩ, while 3-σ deviation is below 1.3 dBΩ. This can be compared to the results published by other authors, although not many works report on Monte Carlo simulation. For example, the work (Atef & Abd-elrahman, 2014) demonstrated the standard deviation of the gain to be below 1.5 dBΩ for the input-stage TIA. This confirms that our proposed design with standard deviation of around 0.4 dBΩ is within the results reported in the literature and we did not sacrifice the robustness of the design for better FOM numbers. Clearly, the distribution is a bit skewed with longer tail towards lower gain. Similar results can be obtained for other gains configurations with relative deviation consistently staying below 7% of the nominal gain.

3.7. Implementation with Cascode Source Follower

Both implementations (correspondingly in CMOS and BiCMOS) above employed the non-cascode configuration for I_{SS}, where two tuning knobs are used for the gain adjustment. In Chapter 2 we have also proposed an improved implementation of a novel alternative configuration with the cascode I_{SS}. The cascode configuration uses larger effective r_{DS} and only single C_1 can be, at least in theory, used for the gain adjustment. The results of the post-layout simulation for the TSMC 0.18 µm CMOS implementation are shown in Fig. 3.17.

While proposing this design improvement we made an assumption that our developed model for Z_{T} should hold in general and the difference shall be only observed in the parametrization of the design. Unfortunately, this is only partially true. Yes, indeed the general expression for Z_{T} still holds as described in Chapter 2. However, the linear scaling scheme as suggested for two tuning knobs does not work well and the parameters of the circuit need manual and non-trivial adjustment. Nevertheless, the Cadence simulation results for the base configu-

ration of Z_{T} = 10 kΩ are superior to those obtained with non-cascode version. The pass-band is extremely flat over the complete bandwidth. Even though the gain is only slightly better (82 dBΩ), the noise level drops far below 1.0 pA/$\sqrt{\text{Hz}}$ which is a tremendous improvement over the previous design. An interesting observation can be seen when one compares the mechanism on how the lower and upper cut-off frequencies are adjusted. In the previously discussed non-cascode implementation the lower cut-off frequency was kept constant, while the upper cut-off frequency was decreasing with an increasing gain. In the suggested cascode realization, however, both cut-off frequencies significantly change with the gain. While, as expected, higher cut-off frequency is again moving towards lower frequencies with increasing gain, the lower cut-off frequency is itself increasing, resulting in alternative bandwidth adjustment pattern. Clearly, further research is needed if one desires such low-noise programmable-gain implementation with constant lower cut-off frequency.

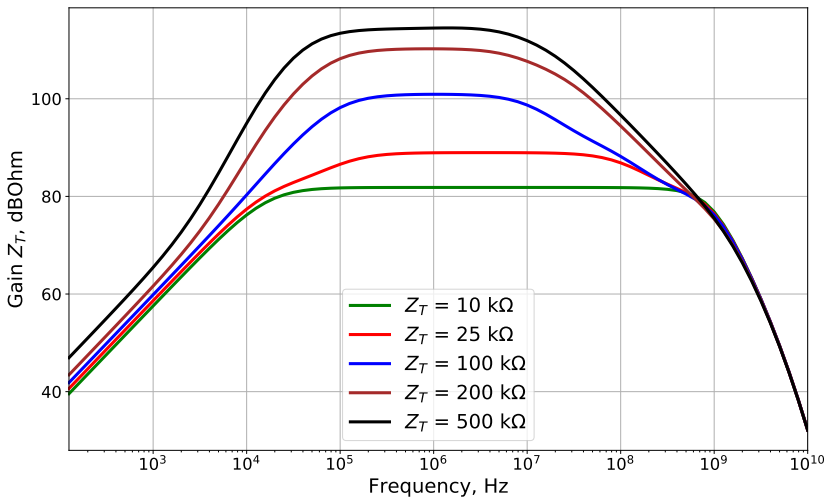

Fig. 3.17. Cadence simulated transimpedance gain for programmable-gain TIA configuration with cascode I_{SS} in TSMC 0.18 µm CMOS

As the application of a linear C_1 and $R_{\mathrm{bias},1}$ scaling with the gain cannot be applied here, only Cadence post-layout simulation is shown. Note that in simulation we still used the linear scaling for the parameter adjustment to get different gains, but comparison with the non-cascode implementation shows that parameter adjustment in programmable-gain concept may need a revision for the version with cascode. As the gain scaling model does not hold for the configuration with cascode, we do not provide here any qualitative measures on fit between the model and the Cadence simulation. Finally, let us consider the very similar cas-

code programmable-gain configuration designed and implemented for 0.25 µm BiCMOS from IHP Microelectronics (Germany). Here, in principle, applies the most of our previous discussion for the equivalent CMOS implementation. While it becomes possible to tune the design to provide extremely flat pass-band, there are still modeling issues, because the manual adjustment of the most important circuit parameters is necessary and linear $R_{\mathrm{bias},1}$ and C_1 scaling scheme, originally proposed for non-cascode configuration, cannot be applied here.

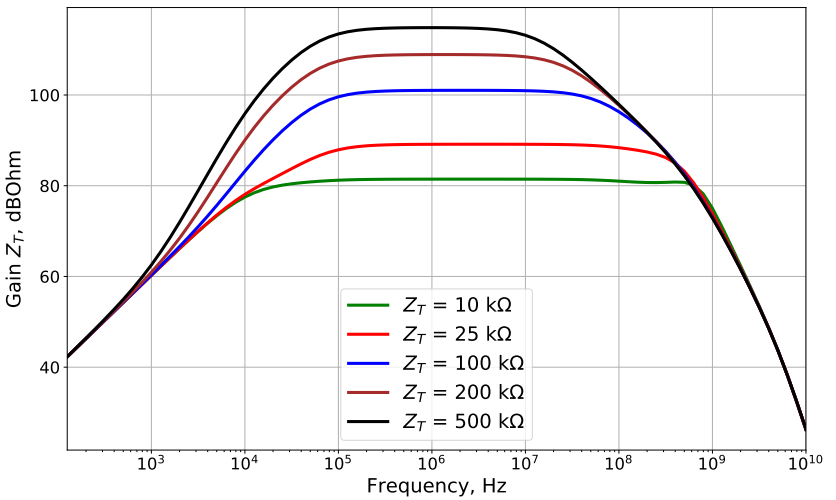

Fig. 3.18. Cadence simulated transimpedance gain for programmable-gain TIA configuration with in IHP 0.25 µm BiCMOS

The previously described noise performance of non-cascode implementations can be also compared to those of the programmable-gain implementations with cascode I_{SS}. The results obtained with TSMC 0.18 µm CMOS are shown in Fig. 3.19), while those obtained with IHP 0.25 µm BiCMOS are presented in Fig. 3.20. As we already discussed in Chapter 2, the implementation with $M_{5\mathrm{C}}$ cascode transistor results in much larger r_{DS5} value. Along with a significant increase of $R_{\mathrm{bias},1}$ value, the circuit is capable to demonstrate lower noise levels, not reachable for non-cascode I_{SS} implementation. For example, for the configuration with Z_{T} = 10 kΩ, the noise minimum decreases from approximately 1.6 pA/$\sqrt{\mathrm{Hz}}$ - 1.8 pA/$\sqrt{\mathrm{Hz}}$ in the case of non-cascode configuration (CMOS and BiCMOS) to around 0.6 pA/$\sqrt{\mathrm{Hz}}$ in the case of cascode-based configuration. This is a tremendous performance improvement in terms of noise at a price of larger r_{DS5}. The BiCMOS-based implementation also demonstrates constant input noise current density over wide frequency range for the two configurations with the largest gain when compared to CMOS-based implementation. Note that all four configurations

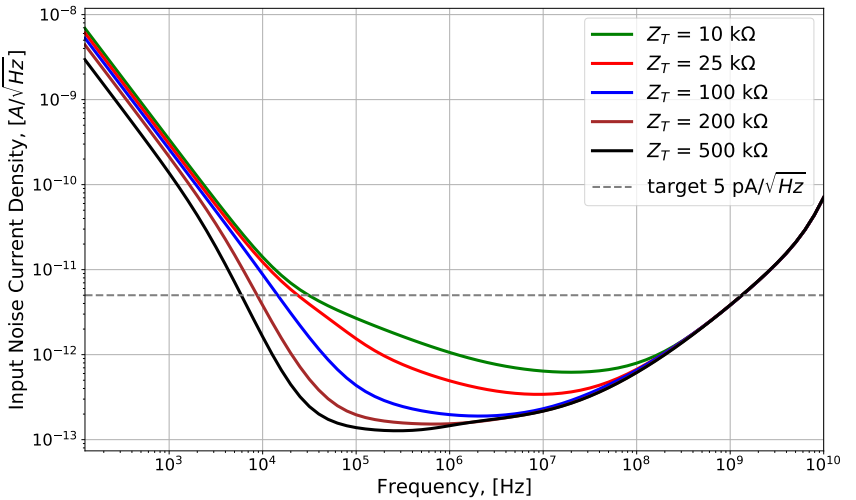

Fig. 3.19. Cadence simulated noise for programmable-gain TIA configuration with cascode I_{SS} in TSMC 0.18 µm CMOS. Horizontal gray dashed line indicates the target noise level of 5.0 pA/$\sqrt{\mathrm{Hz}}$

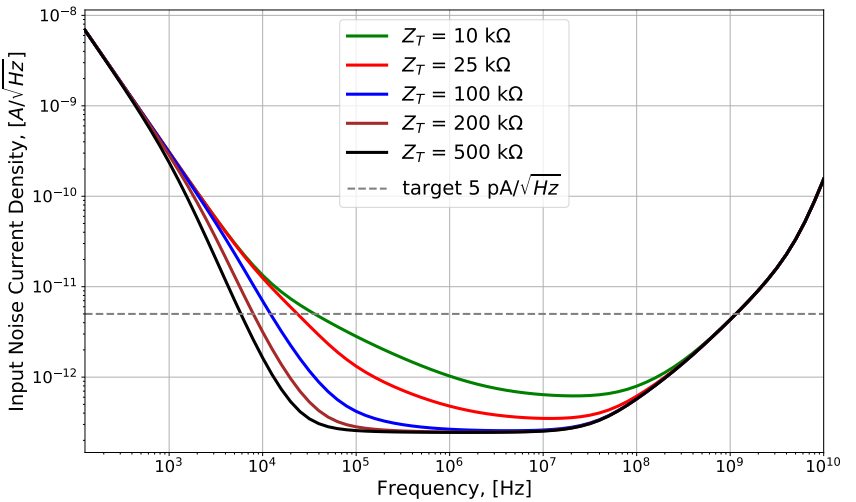

Fig. 3.20. Cadence simulated noise for programmable-gain TIA configuration with cascode I_{SS} in IHP 0.25 µm BiCMOS. Horizontal gray dashed line indicates the target noise level of 5.0 pA/$\sqrt{\mathrm{Hz}}$

(CMOS and BiCMOS, with I_{SS} cascode and without) demonstrate the noise level for the base gain configuration with Z_{T} = 10 kΩ below 2.0 pA/$\sqrt{\mathrm{Hz}}$ which gives us a sufficient noise margin with respect to the OTDR requirement of being below 5 pA/$\sqrt{\mathrm{Hz}}$. As expected, TIA configurations with higher gain result in smaller noise at the price of reduced bandwidth.

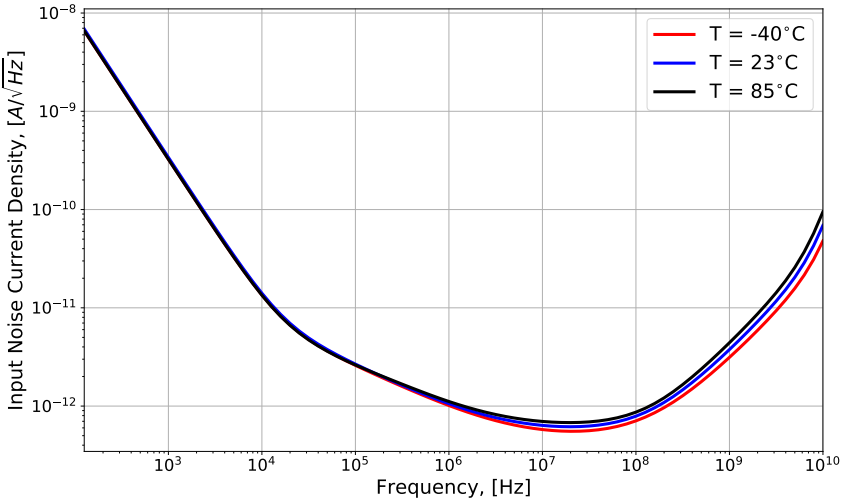

Fig. 3.21. Cadence simulated noise for programmable-gain TIA configuration with cascode I_{SS} in TSMC CMOS and different temperatures

Even though there is rather insignificant variation of the transimpedance gain with temperature (here we consider industrial temperature range as specified in Table 1.3), one may still expect some temperature dependency of the input-referred current noise density as many noise components have an explicit temperature behavior with noise density proportional to the absolute temperature. Fig. 3.21 shows the simulated input-referred noise current for the 10 kΩ TIA in TSMC CMOS. As expected, minor temperature dependency can be seen with slightly increasing impact of temperature towards higher frequencies. An increase of the temperature impact with the frequency can be explained by the structure of the thermal noise components due to R_2 and M_1, where the impact of both noise components increases with frequency due to inverse dependence on transimpedance gain and input impedance correspondingly. The plot confirms, that even if we consider possible increase in noise levels with the temperature, the observed noise is still below the required noise level of 5.0 pA/$\sqrt{\mathrm{Hz}}$ over the target operating temperature range (see Table 1.3). Similar temperature dependency can be shown for other three implementations (BiCMOS and two non-cascode versions). Since the configurations with larger gain also have smaller noises, the absolute impact of the temperature

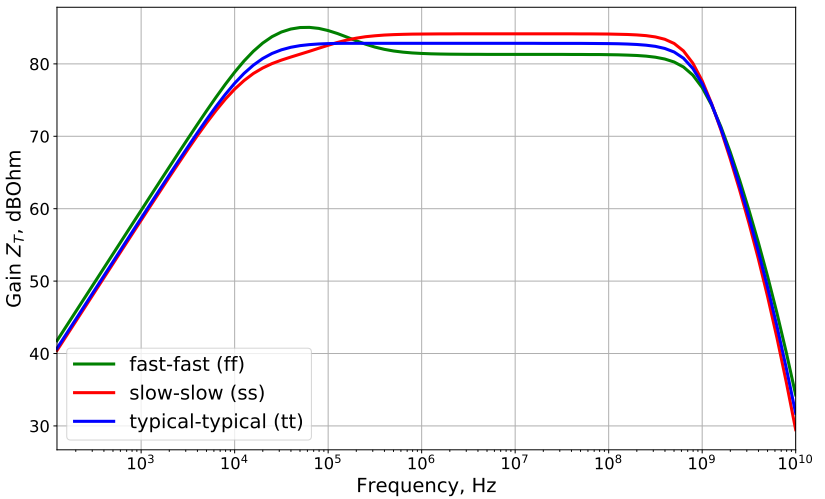

Fig. 3.22. Corner analysis for the transimpedance gain in the case of TSMC 0.18 µm CMOS implementation with cascode I_{SS} and Z_{T} = 10 kΩ

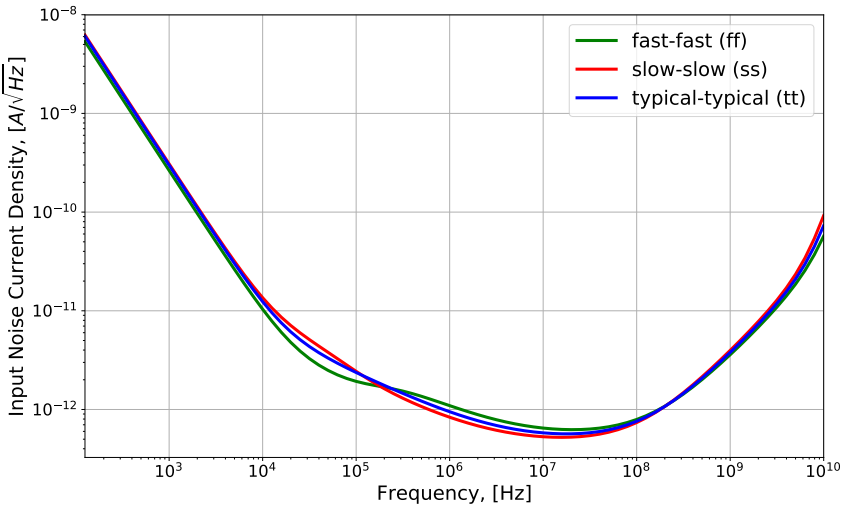

Fig. 3.23. Corner analysis for the noise current density in the case of TSMC 0.18 µm CMOS implementation with cascode I_{SS} and Z_{T} = 10 kΩ

on the noise performance for larger gains is also below the required 5.0 pA/$\sqrt{\text{Hz}}$.

Similarly to the case of non-cascode implementation, we can also perform the corner analysis for the gain and noise as shown in Fig. 3.22 and Fig. 3.23. In the case of the gain, the performance is fundamentally different when compared to non-cascode version shown in Fig. 3.14 for the very same conditions. Here the fast-fast version results in a peak and one clearly sees the absence of the two-region structure within the gain plateau. This, however, can be easily explained by a different structure of the gain model with much larger effective r_{DS5} as already discussed in Chapter 2. Interestingly, there is a stronger change in gain over the entire passband, while in the non-cascode case only upper part of the plateau was affected. This also, at least partially, confirms our observation that the cascode implementation can be considered as a special case of our general architecture with the region transition point moved to very low frequencies. The impact on the noise current seems to be also stronger, but here one has to bear in mind that the overall noise level of the cascode implementation is anyway much smaller when comparing to the non-cascode version and the general noise performance for all corner cases is still fine with respect to the OTDR requirements.

3.8. Discussion

Above we have proposed and evaluated the design methodology for both fixed-gain and programmable-gain CMOS TIA suitable for OTDR applications. The results of simulation confirmed that the proposed design is able to achieve the required gain and bandwidth without any additional stage of post-amplifier. This is an important feature as the solutions with additional stages often consume more power (Jin & Hsu, 2008b) and the stability of them may be compromised (Abd-elrahman et al., 2016). Finally, complex designs may also result in increased noise compared to simpler designs with fewer active elements. Moreover, no inductive peaking was employed to achieve the required gain-bandwidth product and therefore we are able to demonstrate a flat frequency response over the bandwidth of interest with a minimal design footprint. Clearly, the proposed designs cannot compete with high-speed multi-stage implementations using inductive peaking such as those reported in (Jin & Hsu, 2008a,b), where the requirements on the phase linearity, gain ripple and total power consumption may be loosened to achieve very large gain-bandwidth products.

The relative performance of the proposed design for the base configuration with 10 kΩ gain and bandwidth of 1 GHz against a number of selected works and the original performance specification (power 50 mW and noise 5.0 pA/$\sqrt{\text{Hz}}$) is shown in terms of the FOM in Fig. 3.24 and Fig. 3.25 correspondingly as a function of the publication year and the technological node used for the design. The design

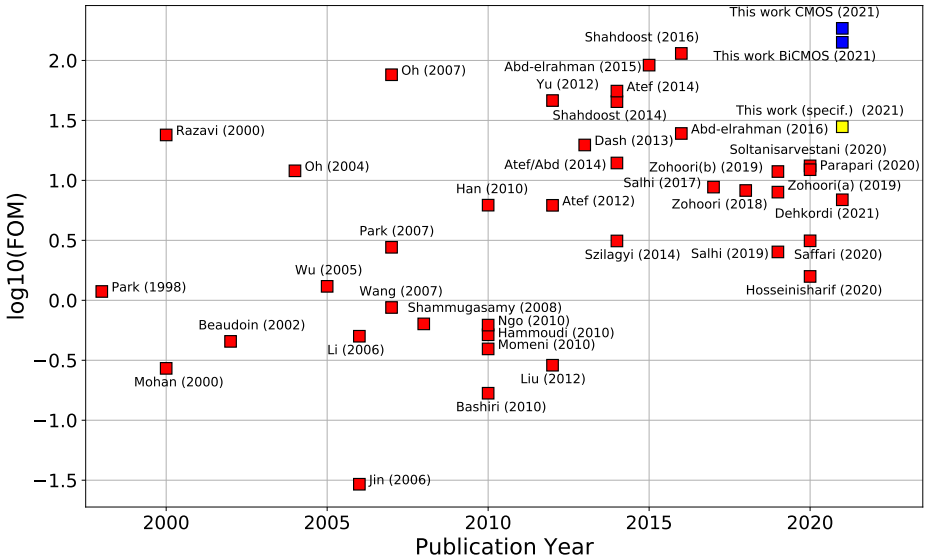

Fig. 3.24. Figure-of-Merit for CMOS TIA as a function of the publication year including the requirements (in yellow) and the proposed designs (in blue) with FOM equal to 185 for CMOS implementation and FOM equal to 141 for BiCMOS implementation

as suggested in our work reaches the value of FOM as high as 185 with an area-efficient inductor-less implementation and the value is close to the performance of TIA reported by (Shahdoost et al., 2016) and (Abd-elrahman et al., 2015). Note that both competing designs were implemented with the more advanced and therefore more expensive 130 nm CMOS process. The proposed design also demonstrates significant improvement over the original specification due to both less consumed power (21 mW vs. 50 mW for CMOS) and lower noise (1.8 pA/$\sqrt{\text{Hz}}$ vs. 5.0 pA/$\sqrt{\text{Hz}}$). We clearly see that the performance of the proposed design is above to the best-published results while using less advanced technological process (0.18 µm, see Fig. 3.25) and we also may expect automatic performance improvement of the amplifier when implemented and tuned for 130 nm or above. Similar performance gain with more advanced technology was demonstrated in (Shahdoost et al., 2016) with similar designs implemented correspondingly with 0.18 µm and 0.13 µm CMOS. Our proposed implementation in BiCMOS reached only FOM equal to 141 due to slightly decreased bandwidth (0.9 GHz vs. 1.0 GHz) and increased power consumption (29 mW vs. 21 mW). Note that this is still better than the work of (Shahdoost et al., 2016) while using even older 0.25 µm technology. Finally, the cascode-based implementation in BiCMOS (not shown) is able to reach as high FOM as 317. Such a huge improvement over the best reported works

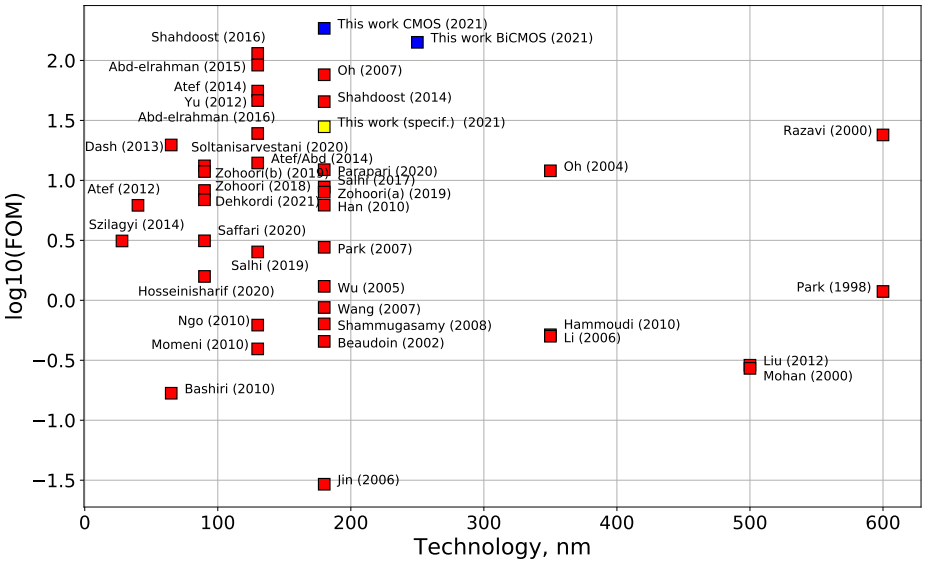

Fig. 3.25. Figure-of-Merit for CMOS TIA as a function of the technological CMOS node including the requirements (in yellow) and the proposed design (in blue) with FOM equal to 185 for CMOS implementation and FOM equal to 141 for BiCMOS implementation

is mainly due to further decrease in noise to the values below 1.0 pA/$\sqrt{\text{Hz}}$ within the bandwidth of interest. Even larger improvement in terms of FOM is possible when implemented in less power-hungry CMOS. As we have mentioned before, the major disadvantage of this modification is a less clear scheme for the parameter adjustment with the gain. As the analytic model for this advanced circuit does not result in a simple schema for the gain adjustment (or, at least, this schema is not known to use at the moment), this preliminary result is not shown in the FOM plots and further work on the topic is needed.

For comparison we have also analyzed the proposed design using the FOM function originally suggested by (Atef & Abd-elrahman, 2014). Here again our suggested capacitive feedback TIA in CMOS proved to be superior to other designs (plots are not shown), where the second best result was reported by older work (Oh & Park, 2007) due to its superior gain-bandwidth performance, but relatively poor noise. This confirms that the superior performance of our design is consistent and independent on whether we take a square root of the bandwidth or not. Still, we see that old FOM as suggested in the series of works of Atef would not allow us to select a capacitive feedback architecture due to a clear preference for higher gain-bandwidth products instead of prioritizing lower noise values.

Within this work we also developed more accurate mathematical models both for the transimpedance gain and input-referred noise current density and compared the model predictions to the results obtained from Cadence post-layout simulations. For the programmable-gain TIA without cascode in source follower we were able to demonstrate only 5% mismatch in gain (in terms of dBΩ) within the bandwidth of interest (up to 1 GHz), while the accuracy of the noise model was around 15% at frequency 500 MHz for configuration Z_{T} = 10 kΩ. The detailed model for transimpedance gain was used to derive several approximate expressions, including new ones, valid for description of TIA in low-frequency range. Further directions for circuit improvement have been indicated with suggested cascode architecture for the current source in source follower block. The proposed modification allows to get extremely flat pass-band and further decreases the achievable noise when compared to our original architecture.

With regard to the FOM performance of the work of (Shahdoost et al., 2016), no details on C_{T} have been specified and the default value of 0.5 pF was used for FOM calculation. The importance of knowing an exact value of assumed or used C_{T} is due to its direct relationship to the major TIA parameters such as bandwidth and gain as much better values of both are typically obtained for smaller input capacitance. This effect is often employed in high-speed CMOS TIA (e.g. for 40 Gbs applications) where small values of C_{T} in the range of 0.05 pF are adopted. In our case, however, the TIA's ability to operate with large values of C_{T} is a specific requirement coming from the OTDR specification as an external PD is employed in the system for improved responsivity. One may also notice that the suggested topology does not result in an extremely low-power circuit when compared to some alternative solutions. However, the original OTDR specification for the power consumption being below 50 mW is fulfilled with a significant margin and we intentionally did not target low power TIA while prioritizing other performance indicators such as gain, bandwidth and noise. Nevertheless, the actual performance in terms of the drawn power provides some space for further circuit improvements or modifications. For example, one still has sufficient available power margin to implement the differential TIA using similar topology[1], employ more advanced configurations for the core voltage amplifier similar to those adopted in Hu et al., (2010a,b) or adjust the circuit for different power/noise ratios. Due to lower noise and ability to operate with larger C_{T} (although this is assumed as no information is provided in works of Shahdoost) our proposed design results in larger value of FOM, while our lower bandwidth and higher power consumption is compensated by larger gain achieved in the proposed design (10 kΩ vs. 6.3

[1] As we have a single channel application and consider solely TIA design and under assumption that the feed-through capacitance is not serious, a decision has been made to implement a single-ended structure for both saving power and transistor/pin count.

kΩ). Still this performance comparison shall be taken with a grain of salt due to uknown C_{T} in works of Shahdoost and the fact that the author reported the numbers for the manufactured and measured circuit, while we report the results of the post-layout simulation. It is also interesting to note the performance of the relatively old work of Razavi (year 2000). Clearly being inferior to some newer works, back in 2000 and with 600 nm it had demonstrated a clearly superior performance outperforming works reported within 7 years after the original publication, where only a switch to a more advanced 0.18 μm process helped to beat the record set by Razavi. We shall also mention that exactly the work of Razavi introduced the original concept of capacitive feedback TIA and this also confirms the superiority of the approach over more conventional techniques even when using older technological nodes.

The proposed programmable-gain capacitive feedback TIA with double control (namely $R_{\mathrm{bias},1}$ and C_1) can be compared to a constant-bandwidth variable-gain fully-differential SFB TIA for RF overlay downstream communication systems reported in (Royo et al., 2016). The proposed design consisted of two cascaded differential pairs with a double control of both the transimpedance and the open-loop gain. The design employed the feedback resistor R_{F} with the transimpedance adjusted to maintain the constant output average power and a linear behavior for all the input ranges and to prevent the amplifier saturation, while the open-loop gain is controlled with a variable load resistor in the first differential pair. In order to implement a variable feedback resistor with maximum linearity, the authors in (Royo et al., 2016) suggested an implementation with a parallel combination of the resistor and a digitally controlled PMOS transistor array (6-bit binary scaled to achieve an 18 dBΩ range with 0.5 dB steps). According to the authors, this strategy maximizes the overdrive voltage with the transistors operating in the ohmic region and the linearity of the TIA is improved. It also improves the dynamic range, and a similar implementation was suggested for the variable load resistor. Compared to this approach, our proposed design has smaller noise (factor 3) and larger gain (80 dBΩ vs. 65 dBΩ) which may be attributed to a general superiority of the capacitive feedback design when compared to resistive SFB TIA employed by the authors. Note also that under a single control case the amplifier reported (Royo et al., 2016) becomes underdamped and high-frequency peaking is produced. This effect is different from the double control scheme proposed in our work, because a clear frequency range separation for both C_1 and $R_{\mathrm{bias},1}$ is possible and this can be seen as a clear advantage of the suggested design methodology. We did not target to implement a constant-bandwidth TIA as this may be not plausible bearing in mind much higher gains when compared to the work of Royo et al., (2016).

The only known to us attempt to implement some variable gain using capacitive feedback TIA was reported in (Yiling Zhang et al., 2008), where an amplifier

Table 3.3. Design target specification, results of current work and selected works with the best reported FOM

Work	R_{T}, [dBΩ]	BW, [GHz]	Noise, [pA/$\sqrt{\mathrm{Hz}}$]	P, [mW]	FOM
Design Target Spec.	80.0	1.0	5.0	50.0	28.0
This work CMOS	80.3	1.0	1.8	21.0	**185**
This work BiCMOS	80.2	0.9	1.6	29.3	141
Yu et al., (2012)	76	1.76	2.67	13.7	114
Shahdoost et al., (2016)	82.3	1.8	0.8	118	46
Abd-elrahman et al., (2015)	61.6	2.0	12.4	3.0	91

was introduced for optical wireless communication links. The capacitive feedback TIA employed a self-biased AGC and it had been claimed that the performance is insensitive to large variations of the input capacitance. The reported TIA-LA achieved a maximum gain of 66 dBΩ, -3 dB bandwidth of 540 MHz at 5 pF detector capacitance and variable gain from 53 dBΩ to 42 dBΩ without instability. The gain element of the core amplifier was defined by a triode-mode PMOS in parallel with R_2 which, according to the authors, results in more linear resistance with tuning. The most important parameters of this circuit such as achievable baseline gain, bandwidth and noise are inferior to those of the approach proposed in our work. The applicability of the simplistic model developed in (Yiling Zhang et al., 2008) for a larger range of circuit parameters is unclear as it ignores not only the value of C_1, but also the impact of the biasing circuits as explained above. Finally, our approach implements a double control strategy with an independent adjustment of the low- and high-frequency performance, while in (Yiling Zhang et al., 2008) only a single tuning parameter R_2 is available. According to the authors, implementation of the AGC with varying load resistor results in the shift of the DC output voltage preventing the coupling of the circuit to the next stage. The authors introduced an additional DC level correction circuit to set the output voltage level to a nearly constant value. Obviously, this additional relatively complex DC level correction circuit is not needed in our design. On the other hand, the authors were able to demonstrate an extremely low sensitivity of their design to the variation in the input capacitance (drop from 68 dBΩ to 66 dBΩ) from 0.5 pF to 5.0 pF respectively with the bandwidth decrease of only 8.4%. The major parameters of the proposed design as well as those of several selected works are shown in Table 3.3 (see Table 1.1 in Chapter 1 for more works).

3.9. Conclusions of Chapter 3

Research results presented in Chapter 3 address dissertation problem No. 2, raised in Chapter 1 conclusions section. Chapter 3 can be summarized with the following

concluding statements:

1. Using TSMC 0.18 µm CMOS technology a capacitive feedback TIA was designed and its performance was investigated. The design employs PMOS-based biasing circuit for the source follower and demonstrates 1 GHz bandwidth, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ programmable-gain, 1.8 pA/$\sqrt{\text{Hz}}$ input-referred noise current density and power consumption of 21 mW at 1.8 V power supply. The circuit has the figure-of-merit of 185 and occupies an area of (150×160) µm^2.
2. In order to compare the chip footprint of the newly developed PMOS-based biasing circuit to the one of the classical pure resistive implementation, two fixed-gain 10 kΩ capacitive feedback TIAs were designed in TSMC 0.18 µm CMOS. While the area of the TIA with pure resistive implementation was (150×200) µm^2, the PMOS-based implementation has a footprint of (130×70) µm^2 and results in 65% area reduction.
3. Using IHP 0.25 µm BiCMOS technology a capacitive feedback TIA with PMOS-based source follower biasing was designed and its performance was investigated. The design demonstrates 0.9 GHz bandwidth, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ programmable-gain, 1.6 pA/$\sqrt{\text{Hz}}$ input-referred noise current density and power consumption of 29 mW at 2.5 V power supply. The circuit occupies an area of (200×180) µm^2 with the computed figure-of-merit reaching 141.
4. The performance of the developed analytical transimpedance gain and input-referred noise current density models was analyzed by comparing their prediction to the those of the computer-based simulations. The results confirm that new models allow to predict accurately the performance of the designed circuit with the mismatch between analytical models and computer simulation as following: 5% for the transimpedance gain in the frequency range up to 1 GHz; 15% in noise current spectral density at the frequency of 500 MHz and gain Z_{T} = 10 kΩ.

General Conclusions

1. Using the newly developed FOM, a comparative analysis of TIA architectures was performed and it was found that the capacitive feedback TIA architecture is best suited for the development of programmable-gain, wide-band, low-noise integrated amplifiers using modern submicron CMOS and BiCMOS technologies.
2. An original programmable-gain TIA architecture was proposed with gain adjustment implemented using a set of discretely controlled feedback capacitors and resistances in the biasing circuits of the input stage. The suggested design supports an implementation of wide-band and low-noise amplifiers with programmable-gain configurations. An innovative PMOS transistor-based solution for the biasing circuit was developed to replace an area-inefficient resistive biasing with achievable area reduction up to 70% for single-gain configuration.
3. New mathematical models for the transimpedance gain and input-referred noise current density have been suggested for the developed architecture. The models can be used as basis for computing accurately the parameters of the amplifier for the frequency range up to 1 GHz. The mathematical model of the transimpedance gain can be used to isolate and compute the major building blocks of the circuit, while the mathematical noise model allows to isolate the major noise sources and to assess their contribution

to the total spectral density of the current noise. The research confirmed that the discrepancy between the suggested models and the results obtained from computer simulation is: 5% for the gain, measuring this discrepancy in the frequency range up to 1 GHz; 15% current noise spectral density at 500 MHz and gain $Z_{\mathrm{T}} = 10\ \mathrm{k}\Omega$.

4. A capacitive feedback TIA with 1 GHz bandwidth and adjustable gain of 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ was designed and investigated using TSMC 0.18 μm CMOS technology. The proposed design has 1.8 pA/$\sqrt{\mathrm{Hz}}$ noise current density, 21 mW power consumption at 1.8 V power supply, occupies (150 × 160) $\mu\mathrm{m}^2$ area and demonstrates FOM as high as 185.
5. A capacitive feedback TIA with 0.9 GHz bandwidth and adjustable gain of 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ and 500 kΩ was designed and investigated using IHP 0.25 μm BiCMOS technology. The proposed design has 1.6 pA/$\sqrt{\mathrm{Hz}}$ noise current density, 29 mW power consumption at 2.5 V power supply, occupies (200 × 180) $\mu\mathrm{m}^2$ area and demonstrates FOM equal to 141.

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Romanova, A. and Barzdenas, V. (2019). A Review of Modern CMOS Transimpedance Amplifiers for OTDR Applications. *Electronics* 8(10)-1073: 1–33. ISSN 2079-9292. IF=2.412.

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Summary in Lithuanian

Įvadas

Problemos formulavimas

Optiniai tinklai yra interneto ryšio pagrindas. Šviesolaidinė technologija laikoma svarbiausiu būsimos tinklo infrastruktūros kūrimo pagrindu, nes užtikrina ypač didelį pralaidumą (teoriškai beveik iki 50 Tb/s), mažą signalo iškraipymą, mažą galios ir vietos poreikį, mažą medžiagų sunaudojimą bei mažą kainą (Lee & Mukherjee, 2004). Interneto srautui didėjant eksponentiškai ir taikant jį vis įvairesnėms paslaugoms, skatinamas naujų tinklų technologijų kūrimas bei esamų pažanga ir pajėgumų didinimas. Toks spartus optinių ryšio sistemų tobulėjimas lemia ir tinklo įrengimo, stebėjimo, priežiūros ir gedimų analizės įrangos poreikį. Vienas iš dažniausiai naudojamų šviesolaidinės linijos kokybės detekcijos prietaisų yra laiko srities optinis reflektometras (angl. *optical time-domain reflectometer*, OTDR). Šio prietaiso veikimas pagrįstas *Rayleigh* šviesos sklaida skaiduloje, kurioje siunčiant lazerio impulsą dėl sąveikos su optinės skaidulos medžiaga ar defektais joje dalis šviesos atspindima priešinga kryptimi ir detektuojama, nustatant atspindžio priežastį. OTDR esantis optinis imtuvas, susidedantis iš fotodetektoriaus ir pereinamosios varžos stiprintuvo (PVS), atsispindėjusį šviesos signalą verčia srovės impulsu ir integruoja, gaunant sustiprintą įtampos signalą, kuris vėliau diskretizuojamas ir skaitmeniškai apdorojamas. Reflektometro pagrindinius parametrus (dinaminį ir matuojamų signalų diapazoną, nejautrumo zoną) dažnai ir riboja įėjime esantis PVS, t. y. jo stiprinimo koeficientas, triukšmai, dažnių juostos plotis bei kiti parametrai. Dažniausiai šie PVS būna varžinio

grįžtamojo ryšio architektūros tipo, kuri taip pat pasižymi dideliu triukšmu. Todėl siekiant tobulinti ir kurti naujos kartos OTDR sistemas, būtina ieškoti naujų PVS architektūrų ir jų pagrindu projektuoti integrinius grandynus. Dėl šios priežasties disertacijoje nagrinėjama problema yra PVS architektūrų, geriausiai atitinkančių šiuolaikinių laiko srities optinių reflektometrinių sistemų reikalavimus, parinkimas ir jų įgyvendinimas viename luste, taikant šiuolaikines submikronines KMOP ir BiKMOP gamybos technologijas. O pasirenkant architektūras ir projektuojant jų integrinius grandynus, atsiranda būtinybė atlikti tiek kokybinę, tiek kiekybinę analizę bei kurti matematinius modelius, aprašančius PVS veikimą plačiame dažnių diapazone. Problemai išspręsti yra iškeliama ir įrodoma darbinė hipotezė, teigianti, kad, taikant šiuolaikines submikronines KMOP ir BiKMOP gamybos technologijas, talpinio grįžtamojo ryšio PVS architektūros pasirinkimas įgalina sukurti valdomo stiprinimo, plačiajuosčius, mažatriukšmius PVS, integruojant juos į vieną lustą.

Darbo aktualumas

Paskutiniame XX amžiaus dešimtmetyje didžiąją dalį pasaulinio puslaidininkių pramonės augimo lėmė asmeniniai kompiuteriai, tačiau svarbus pokytis įvyko apie 2000 m., kai ryšių sektoriaus pajamos iš puslaidininkių gamybos aplenkė kompiuterių sektorių (Buss, 2002). Šis augimas tęsiasi ir iki šių dienų, nes vis auga daiktų interneto (IoT), debesijos, duomenų perdavimo ir saugojimo paslaugų paklausa ir naudotojų skaičius. Pavyzdžiui, nuo minėtų 2000 m. iki šių dienų interneto naudotojų skaičius pasaulyje išaugo daugiau kaip 10,6 karto iki 5,07 milijardo (STATISTA, 2022). Toks spartus augimas lemia ir didėjantį šviesolaidinio interneto ryšio naudojimą. Šiuo metu šviesolaidinės ryšio sistemos sudaro pasaulio ryšių infrastruktūros stuburą, nes užtikrina didžiąją dalį (daugiau nei 99 %) pasaulinio duomenų srauto (CORDIS, 2022). Tačiau nuolatinis eksponentinis duomenų srauto augimas kelia vis didesnius reikalavimus optinio ryšio kanalui, jo kokybei bei patikimumui. Optinei linijai testuoti dažniausiai taikoma optinė reflektometrija, kurios pagrindu sukurtais OTDR prietaisais įmanoma išmatuoti visus optinės skaidulos parametrus, būtinus tinkamam ryšio kanalo eksploatavimui. Dėl palyginti mažos OTDR prietaisų rinkos apimties juose naudojami PVS yra gaminami panaudojant diskrečiuosius komponentus, leidžiančius pasiekti gana siaurą praleidžiamųjų dažnių juostos plotį, mažesnį nei 100 MHz (Charlamov, 2013; Charlamov & Navickas, 2015). Tokios grandinės pasižymi didelėmis parazitinėmis talpomis, didesne vartojamąja galia, didesniu triukšmu, atsiranda sunkumų norint pasiekti didesnį dinaminį diapazoną bei geresnį signalo / triukšmo santykį (Yeom et al., 2019). Šias problemas sumažinti arba išvis eliminuoti būtų galima įgyvendinus PVS viename integriniame luste. Siekiant sumažinti kainą ir padidinti kuriamų OTDR konkurencingumą, vis dažniau žvelgiama į finansiškai patrauklias, didesnių integravimo galimybių submikronines KMOP ir BiKMOP technologijas su f_{T} dažniu dešimties GHz ribose.

Lietuvoje moksliniai tyrimai, susiję su PVS grandynais, nėra plačiai paplitę. Šia tematika tyrimo rezultatus publikuoja VILNIUS TECH mokslininkai J. Charlamov ir R. Navickas (Charlamov & Navickas, 2015). Taip pat tyrimus sparčiųjų integrinių grandynų srityje atlieka K. Kiela, M. Jurgo, A. Vasjanov, V. Mačaitis, L. Kladovščikov bei Vilniuje ir Kaune įsikūrusios uždarosios akcinės bendrovės „Lime Microsystems“ ir „Si Femto“. Apibendrinant galima teigti, kad šiuolaikiniai PVS nėra pakankamai ištirti ir aprašyti, darbe vykdomi tyrimai yra aktualūs, o gauti rezultatai bei tolimesni tyrimai paspartins naujos kartos laiko srities optinės reflektometrijos matavimo prietaisų vystymąsi.

Tyrimų objektas

Darbo tyrimų objektas – submikroninių KMOP ir BiKMOP gamybos technologijų pereinamosios varžos stiprintuvų (PVS) architektūros ir PVS integriniai grandynai.

Darbo tikslas

Šio darbo tikslas yra, taikant šiuolaikines submikronines KMOP ir BiKMOP gamybos technologijas, sukurti diskretiniu būdu valdomo stiprinimo, plačiajuosčius, mažatriukšmius PVS ir jų integrinius grandynus, skirtus šiuolaikiniams laiko srities optinės reflektometrijos matavimo prietaisams kurti.

Darbo uždaviniai

Darbo tikslui pasiekti buvo sprendžiami šie uždaviniai:

1. Atlikti naujausių PVS architektūrų tyrimus, pateikiant kokybinės ir kiekybinės analizės rezultatus, bei išnagrinėti šių architektūrų tinkamumą šiuolaikiniams laiko srities optinės reflektometrijos matavimo prietaisams kurti.
2. Sukurti originalią talpinio grįžtamojo ryšio ir diskretiniu būdu valdomo stiprinimo PVS architektūrą bei ją aprašančius matematinius modelius, leidžiančius kurti plačiajuosčius ($\geq$1 GHz), mažatriukšmius ($\leq$5,0 pA/$\sqrt{\text{Hz}}$) PVS.
3. Suprojektuoti ir ištirti pasiūlytos architektūros PVS integrinius grandynus, taikant šiuolaikines submikronines TSMC 0,18 μm KMOP ir IHP 0,25 μm BiKMOP gamybos technologijas.

Tyrimų metodika

Talpinio grįžtamojo ryšio PVS architektūroms ir jų integriniams grandynams projektuoti bei tirti taikyti analitiniai, matematiniai ir kompiuterinio modeliavimo tyrimo metodai. Analitiniai metodai buvo taikomi apibendrinant įvairias PVS architektūras, o matematiniai, kompiuteriniai modeliavimo tyrimo metodai – projektuojant ir tiriant talpinio grįžtamojo ryšio PVS integrinius grandynus. Projektuojant šiuos PVS integrinius grandynus buvo panaudotos submikroninės TSMC 0,18 μm KMOP ir IHP 0,25 μm BiKMOP gamybos procesų technologinės bibliotekos. Suprojektuoti PVS buvo modeliuojami ir tiriami taikant profesionalų integrinių grandynų projektavimo *Cadence Virtuoso* programų paketą.

Darbo mokslinis naujumas

Rengiant disertaciją buvo gauti šie elektros ir elektronikos inžinerijos mokslui nauji ir reikšmingi rezultatai:

1. Siekiant kiekybiškai palyginti skirtingų gamybos technologijų ir įvairias PVS architektūras, pasiūlyta nauja kokybės funkcija, apimanti pagrindinius PVS parametrus: praleidžiamųjų dažnių juostos plotį, stiprinimo koeficientą, suminę įėjimo talpą, vartojamąją galią bei triukšminius parametrus.

2. Pasiūlyta nauja ir originali talpinio grįžtamojo ryšio PVS architektūra su PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandine, leidžianti įgyvendinti diskretiškai valdomą stiprinimą, mažus triukšmus (1,8 pA/$\sqrt{\text{Hz}}$) ir ypač plačią praleidžiamųjų dažnių juostą (1 GHz), ši juosta įgalina suprojektupti ir pagamintį PVS grandinę taikant šiuolaikines submikronines KMOP bei BiKMOP integrinių grandynų gamybos technologijas.
3. Pasiūlyti nauji siūlomos PVS architektūros stiprinimo koeficiento bei srovės triukšmo spektrinio tankio matematiniai modeliai, kurie praplečia šių parametrų tikslumą dažnių ruože iki 1 GHz, lyginant su kitų autorių darbais, ir kurių neatitikimas, lyginant su kompiuterinio modeliavimo rezultatais, neviršija: 5 % stiprinimo koeficientui, matuojant šį neatitikimą dažnių juostoje iki 1 GHz; ir 15 % srovės triukšmo spektriniam tankiui, esant 500 MHz dažniui bei 10 kΩ stiprinimui.
4. Taikant šiuolaikines submikronines 0,18 μm KMOP ir 0,25 μm BiKMOP integrinių grandynų gamybos procesų technologijas, suprojektuoti 1 GHz / 0,9 GHz praleidžiamųjų dažnių juostos, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ diskretiniu žingsniu valdomo stiprinimo, 1,8 pA/$\sqrt{\text{Hz}}$ / 1,6 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinio tankio, esant 21 mW / 29 mW vartojamajai galiai ir 1,8 V / 2,5 V maitinimo įtampai, PVS bei ištirti jų pagrindiniai parametrai.

Darbo rezultatų praktinė reikšmė

Disertacijoje gauti rezultatai panaudoti projektuojant PVS integrinius grandynus šiuolaikinėse submikroninėse 0,18 μm KMOP ir 0,25 μm BiKMOP gamybos technologijose. Pasiūlyta kokybės funkcija gali būti naudojama įvertinant skirtingų gamybos technologijų ir architektūrų PVS, o naujai pasiūlyta diskretiniu būdu valdomo stiprinimo, talpinio grįžtamojo ryšio PVS architektūra bei ją aprašantys matematiniai modeliai gali būti panaudoti kuriant šiuolaikinius laiko srities optinės reflektometrijos matavimo prietaisus. Tyrimų metu gauti rezultatai taip pat gali būti taikomi ir kitose optinėse sistemose, kurioms ypač svarbi yra mažų triukšmų, didelio jautrumo ir praleidžiamųjų dažnių juostos problema, bei gali būti akstinas tolesniems PVS ir jų pagrindu kuriamų optinių sistemų tyrimams ir (arba) tobulinimams.

Ginamieji teiginiai

Disertacijos metu yra suformuluoti tokie ginamieji teiginiai:

1. Pasiūlyta nauja kokybės funkcija leidžia atlikti įvairių PVS architektūrų, įgyvendintų KMOP ir BiKMOP gamybos technologijomis, palyginamąją analizę ir matematiškai išskirti kompromisą tarp stiprinimo koeficiento ir praleidžiamųjų dažnių juostos pločio sandaugos bei srovės triukšmo spektrinio tankio, būtiną šiuolaikinėms laiko srities optinėms reflektometrinėms sistemoms kurti.
2. Pasiūlyti stiprinimo koeficiento ir srovės triukšmo spektrinio tankio matematiniai modeliai praplečia siūlomos PVS architektūros šių parametrų tikslumą dažniu ruože iki 1 GHz, o neatitikimas su kompiuterinių modeliavimų metu gautais rezultatais yra: 5 % stiprinimo koeficientui, matuojant šį neatitikimą dažnių juostoje iki 1 GHz; 15 % srovės triukšmo spektriniam tankiui, esant 500 MHz dažniui

ir 10 kΩ stiprinimo koeficientui.

3. Suprojektuotas siūlomos architektūros KMOP PVS leidžia 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ diskretiniu žingsniu valdyti stiprinimą bei užtikrina 1 GHz praleidžiamųjų dažnių juostos plotį ir 1,8 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinį tankį, esant 10 kΩ stiprinimo koeficientui, 21 mW vartojamajai galiai bei 1,8 V maitinimo įtampai.
4. Pasiūlyta diskretiniu būdu valdomo stiprinimo su talpiniu grįžtamuoju ryšiu PVS architektūra gali būti įgyvendinta šiuolaikinėse submikroninėse TSMC 0,18 µm KMOP ir IHP 0,25 µm BiKMOP gamybos technologijose.

Darbo rezultatų aprobavimas

Darbo rezultatai paskelbti septyniuose moksliniuose straipsniuose: dvi publikacijos (Romanova & Barzdenas, 2019a; Romanova & Barzdenas, 2021a) moksliniuose žurnaluose, referuojamuose *Clarivate Analytics Web of Science* duomenų bazėje ir turinčiuose citavimo rodiklius; viena publikacija (Romanova & Barzdenas, 2020a) mokslo žurnale, referuojamame *Clarivate Analytics Web of Science* duomenų bazėje, tačiau neturinčiame citavimo rodiklio; dvi publikacijos konferencijų medžiagose, įtrauktose į *Clarivate Analytics Web of Science* „Conference Proceedings“ duomenų bazę (Romanova & Barzdenas, 2018; Romanova & Barzdenas, 2020c); ir dvi publikacijos (Romanova & Barzdenas, 2019b; Romanova & Barzdenas, 2020b) konferencijų medžiagose, įtrauktose į kitas tarptautines duomenų bazes.

Disertacijoje atliktų tyrimų rezultatai buvo paskelbti penkiose mokslinėse konferencijose Lietuvoje ir užsienyje:

- 21-ojoje Lietuvos jaunųjų mokslininkų konferencijoje „Mokslas – Lietuvos ateitis. Elektronika ir elektrotechnika“, vykusioje Vilniuje 2018 m. kovo 16 d.;
- 2-ojoje tarptautinėje konferencijoje „Electrical, Electronic and Information Sciences 2018 (eStream 2018)“, vykusioje Vilniuje 2018 m. balandžio 26 d.;
- tarptautinėje konferencijoje „IEEE Microwave Theory and Techniques in Wireless Communications (MTTW)“, vykusioje Rygoje, Latvijoje 2019 m. spalio 1–2 d.;
- 4-ojoje tarptautinėje konferencijoje „Electrical, Electronic and Information Sciences 2020 (eStream 2020)“, vykusioje Vilniuje 2020 m. balandžio 30 d.;
- 27-ojoje tarptautinėje konferencijoje „International Conference on Mixed Design of Integrated Circuits and System (MIXDES)“, vykusioje Vroclave, Lenkijoje 2020 m. birželio 25–27 d.

Disertacijos struktūra

Darbą sudaro įvadas, trys skyriai, išvados, literatūros sąrašas ir autoriaus publikacijų disertacijos tema sąrašas. Taip pat yra trys priedai. Darbo apimtis yra 184 puslapių, neskaitant priedų, tekste panaudotos 133 numeruotos formulės, 73 paveikslai ir 6 lentelės. Rašant disertaciją buvo panaudota 115 literatūros šaltinių.

1. Šiuolaikinių pereinamosios varžos stiprintuvų architektūrų ir jų pritaikomumo laiko srities optinėms reflektometrinėms sistemoms analizė

Nors pagrindinės PVS koncepcijos yra tokios pat senos kaip grįžtamojo ryšio stiprintuvų, septintojo dešimtmečio pabaigoje ir aštuntojo dešimtmečio pradžioje PVS plačiau imta naudoti kuriant optines ryšio sistemas (Razavi, 2019). PVS paprastai naudojami tose srityse, kuriose būtina keisti įvairių jutiklių mažas sroves, gaunant įtampą ir vėliau ją apdorojant bei analizuojant. Be optinių ryšio sistemų, PVS taip pat plačiai naudojami MEMS jutiklių nuskaitymo grandinėse (Keshri, 2010; Mekky et al., 2013; Royo et al., 2017; Salvia et al., 2009; Woo et al., 2017), LIDAR (Ma et al., 2018), ypač mažų matmenų magnetinio rezonanso sistemose (Ghanad & Dehollain, 2016), biologinių jutiklių pirminėse grandinėse (Hu et al., 2010a; Wilson & Chen, 2014), ultragarsinio vaizdavimo sistemose (Cenkeramaddi & Ytterdal, 2009; Monsurro et al., 2010), spektroskopijoje (Chaddad & Tanougast, 2014; Rajabzadeh et al., 2018) ir kitose srityse. Akivaizdu, kad šis platus pritaikymo sričių spektras lemia ir skirtingus reikalavimus PVS architektūroms. Tačiau optinėse ryšio sistemoje išryškėja trys pagrindinės parametrų gerinimo tendencijos: stiprinimo koeficiento ir dažnių juostos sandaugos didinimas bei triukšminių parametrų ir vartojamosios galios mažinimas (Shahdoost et al., 2014). Į PVS įėjimą apdorojimui tiekiama fotodiodo generuojama srovė i_{PD} kartu su jo triukšmine srove $i_{\mathrm{n,PD}}$. Todėl PVS yra laikytinas svarbiausiu komponentu, turinčiu įtakos svarbiausioms optinio imtuvo charakteristikoms: jautrumui triukšmams, visos optinės sistemos spartai ir kt. Šias triukšmines charakteristikas atitinka įėjime esantis ekvivalentinio triukšmo srovės generatorius $i_{\mathrm{n,TIA}}$, kurio triukšmo pobūdis priklauso nuo PVS architektūros ir joje naudojamų elementų.

Istoriškai plačiajuosčiai ir mažatriukšmiai PVS buvo kuriami taikant GaAs, InP, HBT, HEMT ir SiGe BiKMOP (Bertenburg et al., 1996) gamybos technologijas. Šios technologijos buvo pasirenkamos dėl puikių triukšminių, greitaveikos ir stiprinimo charakteristikų. Tačiau šiuo metu vis labiau populiarėja submikroninės KMOP technologijos, pasižyminčios didelės integracijos galimybėmis, dideliu ištobulinimo lygiu ir žemomis gamybos kainomis (Atef & Zimmermann, 2012; Razavi, 2002; Yong-Hun Oh & Sang-Gug Lee, 2004).

Mokslinėje ir inžinerinėje literatūroje publikuojama sąlygiškai daug darbų apie įvairios paskirties KMOP technologijų PVS ir jų architektūras. Nors šių publikacijų autoriai beveik visada pateikia gautų pagrindinių parametrų apibendrinimą, kartu su 8 ar 10 konkurentų alternatyvių sprendimų palyginimu, tačiau toks palyginimas nėra labai vaizdus bei neparodo siūlomos architektūros ar grandinės pranašumo. Todėl norint atlikti palyginamąją analizę, būtina sudaryti vieną palyginimo matą, t. y. įvesti bendrąją kokybės funkciją (angl. *Figure of Merit*, FOM), kuri užtikrintų teisingą pusiausvyrą tarp pagrindinių PVS parametrų, tokių kaip praleidžiamųjų dažnių juostos plotis, stiprinimo koeficientas ir kiti parametrai. Nors literatūroje yra bandymų pasiūlyti tokios funkcijos apskaičiavimo metodų (Salhi et al., 2019; Szilagyi et al., 2014), tačiau jie turi savų trūkumų. Pavyzdžiui, minėtame (Szilagyi et al., 2014) darbe neįvertinama C_{D} fotodiodo talpa ir triukšminiai parametrai, kurie yra ypač svarbūs PVS projektavimo kriterijai. Kita vertus, sudėtingos funkcijos, kaip siūloma darbe (Salhi et al., 2019), gali įvertinti net naudojamos technologijos f_{T} ribinį perdavimo dažnį. Tačiau analizuojant literatūrą pastebėta, kad tik labai retai autoriai nurodo f_{T} ir konkrečiai naudojamą technologiją bei jos gamintoją. Neturint šių

duomenų arba esant labai ribotam jų kiekiui, būtų sunku arba net neįmanoma atlikti įvairų architektūrų PVS palyginamąją analizę. Taip pat į kokybės funkcijos išraišką būtų galima įtraukti ir užimamą plotą luste, tačiau dažniausiai mokslo publikacijose nurodomas visas lusto plotas, į kurį, be PVS, įtraukiamas ir kitų grandinių užimamas plotas. Atkreiptinas dėmesys, kad ne visuose moksliniuose tyrimuose stengiamasi sumažinti galutinės grandinės topologijos plotą, nes dažnai pagrindinis tikslas yra pagerinti PVS charakteristikas bei parodyti siūlomų architektūrų privalumus, o tai savo ruožtu dažnai neatitinka pramonės gaminiams keliamo kokybės lygio. Todėl, siekiant palyginti skirtingų architektūrų ir panaudojimo sričių PVS, šioje disertacijoje siūloma tokia kokybės funkcijos matematinė išraiška:

$$FOM = \frac{\sqrt{BW\,[\mathrm{GHz}]}R_{\mathrm{T}}\,[\Omega]\,C_{\mathrm{T}}\,[\mathrm{pF}]}{Noise\left[\mathrm{pA}/\sqrt{\mathrm{Hz}}\right]\,P[\mathrm{mW}]}. \tag{S1.1}$$

Šioje išraiškoje P yra vartojamoji galia mW, C_{T} suminė įėjimo talpa, išreikšta pF, BW yra PVS praleidžiamųjų dažnių juostos plotis GHz, R_{T} stiprinimo koeficientas žemuosiuose dažniuose, išreikštas Ω, ir $Noise$ – srovės triukšmo spektrinis tankis pA/$\sqrt{\mathrm{Hz}}$. Atkreiptinas dėmesys, kad šioje išraiškoje imama BW kvadratinė šaknis, siekiant tikslesnio palyginimo su srovės triukšmo spektriniu tankiu. Iš šios išraiškos matyti, kad PVS, turintys didesnius BW, R_{T}, ir C_{T}, didina šį įvertį, o $Noise$ ir P mažina. Remiantis minėta kokybės funkcija, atlikta skirtingų architektūrų ir panaudojimo sričių PVS analizė, kuri leido išskirti kelias pagrindines architektūras. Taip pat reiktų paminėti ir tai, kad siūloma kokybės funkcijos išraiška turi dimensiją, bet analitinėje analizėje rodoma be jos, t. y. tik skaitinė jos reikšmė, siekiant supaprastinti palyginimą.

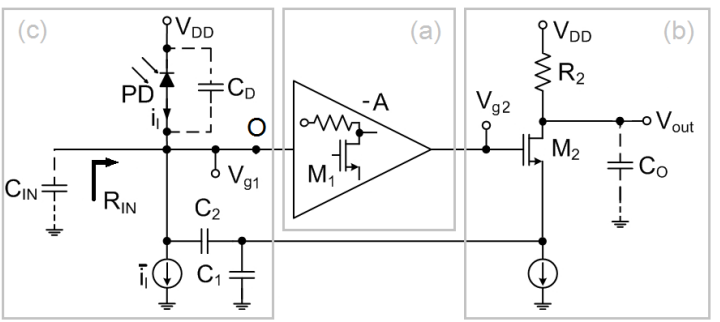
Vienas iš pagrindinių klasikinio varžinio grįžtamojo ryšio PVS trūkumų yra prastos triukšminės charakteristikos nes grįžtamojo ryšio rezistoriaus triukšmas yra sumuojamas su suminio įėjimo srovės triukšmo spektriniu tankiu. Taigi, vienas iš galimų sprendimų, sumažinantis PVS grandinės triukšmą, yra pakeisti triukšmingą grįžtamojo ryšio rezistorių kitu netriukšmingu komponentu – kondensatoriumi ar jų grandine. Tokia grandinė pašalintų tipinio varžinio grįžtamojo ryšio trūkumus, išlaikant grandinės grįžtamojo ryšio struktūros privalumus. Bandymas spręsti triukšmines PVS architektūrų problemas, naudojant talpinį grįžtamąjį ryšį, pirmą kartą buvo aprašytas (Razavi, 2000) darbe ir išplėtotas darbų serijoje (Shahdoost et al., 2014; Shahdoost et al., 2014, 2011, 2016). Ir kaip matyti iš disertacijoje pateiktos analizės, didžiausią ir labiausiai išsiskiriančią kokybės funkcijos reikšmę turi (Shahdoost et al., 2016) darbe pateikiamas PVS, kuris siekia net 114,4. Šis autorių siūlomas PVS yra būtent talpinio grįžtamojo ryšio. Todėl dėl tokio ryškaus kokybės funkcijos skirtumo tarp skirtingų architektūrų PVS, pagamintų taikant KMOP ir BiKMOP technologijas, šioje disertacijoje išsamiai tyrinėjama talpinio grįžtamojo ryšio architektūra ir jos pagrindu kuriamas naujas bei originalus, diskretiškai valdomo stiprinimo, plačiajuostis, mažatriukšmius PVS.

Atlikus mokslinių publikacijų ir komercinių produktų analizę, apskaičiuotas ir sudarytas pagrindinių PVS parametrų rinkinys, kurį schemotechniškai įgyvendinus viename luste ir naudojant KMOP bei BiKMOP technologijas, būtų galima kurti šiuolaikinius optimalių parametrų laiko srities optinės reflektometrijos matavimo prietaisus. Yra nustatyta, kad praleidžiamųjų dažnių juosta turi būti apie 1 GHz, įvertinant reflektometro nejautrumo zoną. Matuojant -45 dB atspindžio koeficientą turintį įvykį su 1 ns trukmės lazerio impulsu, kai optinio imtuvo dažnių juosta lygi 1 GHz, būtų gauta 0,3 metro ilgio nejautrumo zona,

kuri būtų mažesnė už šiuo metu pasiektą ir naudojamą rinkoje (LUCIOL, 2021, 2022). Reflektometro dinaminį diapazoną, nulemia PVS triukšminiai parametrai ir stiprinimo koeficientas (Charlamov, 2013). Tačiau šie modeliai yra skirti klasikinei varžinio grįžtamojo ryšio PVS architektūrai ir dėl kelių stiprintuvo parametrų bendros sąveikos nėra tikslūs ir tinkami talpinio grįžtamojo ryšio PVS. Todėl darant pagrįstą prielaidą, kad talpinio grįžtamojo ryšio PVS triukšmų lygis yra mažesnis nei klasikinės PVS architektūros, galima apytiksliai įvertinti triukšmo lygius, pasiekiamus tiksliniam 1 GHz dažnių juostos pločiui. Pavyzdžiui, Shahdoost darbų serijoje buvo įrodyta, kad, naudojant talpinio grįžtamojo ryšio PVS, galima pasiekti maždaug 3 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinį tankį. Todėl šioje disertacijoje mes nusistatėme 5 pA/$\sqrt{\text{Hz}}$ viršutinę ribą visame dažnių juostos plotyje, nes toks triukšmo lygis turi būti įmanomas pasiekti kruopščiai suprojektuotai grandinei. Taip pat šioje disertacijoje siūloma naudoti ir panašias 0,18 µm KMOP bei 0,25 µm BiKMOP gamybos technologijas, nes jos turėtų leisti pasiekti reikiamą stiprinimą, triukšmo lygį bei pralaidumo juostos plotį panaudojant mūsų pasirinktą PVS architektūrą. Kiti šios specifikacijos parametrai gauti iš geriausių publikuojamų mokslinių straipsnių rezultatų.

2. Talpinio grįžtamojo ryšio pereinamosios varžos stiprintuvų modelio kūrimas ir tyrimas

Antrajame disertacijos skyriuje išsamiai aprašoma naujai siūloma originali, diskretiškai valdomo stiprinimo talpinio grįžtamojo ryšio PVS architektūra bei pateikiami nauji matematiniai modeliai, aprašantys pagrindinius PVS parametrus. Visą talpinio grįžtamojo ryšio PVS architektūrą galima būtų atvaizduoti supaprastinta struktūrine schema (S2.1 pav.).



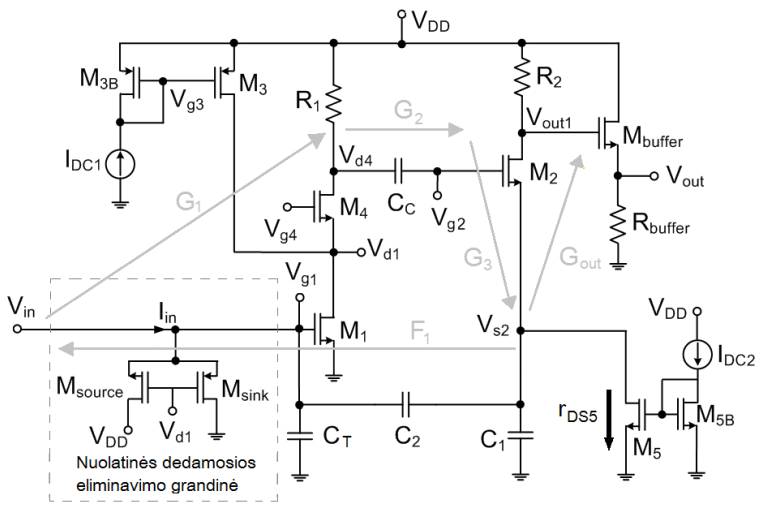
S2.1 pav. Talpinio grįžtamojo ryšio PVS struktūra su pagrindiniais blokais: pagrindinio stiprinimo (a), išėjimo ištakos kartotuvo (b) ir grįžtamojo ryšio (c)

Šioje architektūroje C_2 kondensatorius nustato įtampą ant pirmojo grįžtamojo ryšio C_1 kondensatoriaus, ir nustatomai įtampai proporcinga srovė grąžinama į stiprintuvo įėjimą. O darant prielaidą, kad G_1 stiprinimas A yra labai didelis, t. y. $A \gg 1$, gaunamas srovės stiprinimas gali būti apytiksliai išreiškiamas kaip $1 + C_1/C_2$. Šis grįžtamasis ryšys gali būti laikomas srovės stiprintuvu ir prijungus prie tranzistoriaus M_2 santakos rezistorių

R_2, PVS stiprinimas R_T žemuosiuose dažniuose teoriškai gali būti aproksimuotas kaip:

$$R_\mathrm{T} = \left(1 + \frac{C_1}{C_2}\right) R_2. \tag{S2.1}$$

Matyti, kad šios architektūros PVS stiprinimą galima valdyti keičiant šių grįžtamųjų kondensatorių santykį. Taip pat šis talpinis stiprinimas nekelia triukšmo, o išėjime esančio rezistoriaus R_2 terminis triukšmas yra sąlygiškai mažas. Tačiau, kaip jau minėjome, ši stiprinimo koeficiento išraiška yra teorinė, o įgyvendinus realiomis grandinėmis matematinis modelis tampa daug sudėtingesnis. Tai mes įrodėme ir verifikavome šioje disertacijoje. S2.2 paveiksle pavaizduota disertacijoje siūloma fiksuoto stiprinimo talpinio grįžta-

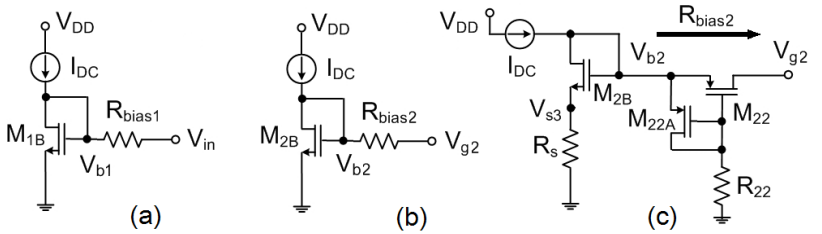


S2.2 pav. Siūloma fiksuoto stiprinimo talpinio grįžtamojo ryšio PVS grandinė

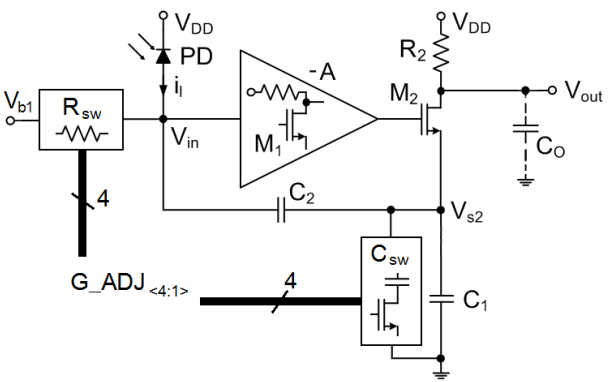
mojo ryšio PVS grandinė. Šioje schemoje, siekiant minimalių triukšminių charakteristikų, pagrindiniam stiprintuvui parinkta vienpakopė bendrosios ištakos konfigūracija. Ši konfigūracija papildyta M_4 tranzistoriaus kaskodu, kuris yra skirtas nustatyti M_1 tranzistoriaus darbo tašką. Grandinės stiprinimas yra padidintas panaudojant stiprinimo skatinimą su papildomu M_3 PMOP tranzistoriumi. M_2 kartu su R_2 bei srovės veidrodžiu M_5/$M_{5\mathrm{B}}$ atitinka ištakos kartotuvo konfigūraciją. M_source ir M_sink tranzistorių jungimas skirtas fotodetektoriaus nuolatinės srovės dedamajai eliminuoti.

Įgyvendinant siūlomos architektūros PVS grandinę, dideliu inžineriniu iššūkiu tampa įtampos atsargos (angl. *voltage headroom*) užtikrinimas atraminių priešįtampių kūrimo srityje. Ši problema tampa ypač aktuali naudojant 0,18 µm KMOP ir 0,25 µm BiKMOP technologijas, kurių maitinimo įtampos yra palyginti žemos (pvz., 1,8 V ar 2,5 V). Iššūkius kelia dvi atraminio priešįtampio grandinės M_1 ir M_2 tranzistoriams, jos S2.2 paveiksle atitinka V_in arba V_g1 ir V_g2. V_in atraminio priešįtampio grandinė, esanti visos grandinės įėjime, turi būti parinkta taip, kad užtikrintų kuo mažesnius patenkančius triukšmus ir įėjimo talpas. Tinkamam šios PVS grandinės veikimui šis atraminis priešįtampis turi būti apie 0,7 V. Tokią įtampą galima pasiekti naudojant visiškai varžinio pobūdžio grandinę,

kuri pavaizduota S2.3 pav., (a), nes PVS konfigūracijai, kurios stiprinimo koeficientas R_{T} = 10 kΩ, $R_{\mathrm{bias},1}$ turi būti tik 17 kΩ. Toks varžos dydis sąlygiškai mažas, neturintis didelės įtakos triukšminiams parametrams ir užimam plotui luste. Tačiau tokia visiškai varžinio atraminio priešįtampio grandinė nėra tinkama V_{g2} įgyvendinimui (S2.3 pav., (b)). Su siūloma PVS grandine siekiant pasiekti bent 100 kHz žemutinę praleidžiamųjų dažnių juostos ribą, šis atraminis priešįtampis turi būti apie 1,2 V, o tai lemtų net MΩ eilės $R_{\mathrm{bias},2}$ rezistorių, esant tam pačiam R_{T} = 10 kΩ stiprinimui. Tokios didelės vertės $R_{\mathrm{bias},2}$ įgyvendinimas lemtų labai didelį užimamą plotą luste. Šiai problemai spręsti pasiūlyta nauja PMOP tranzistorių pagrindu įgyvendinta V_{g2} atraminio priešįtampio grandinė, kuri pavaizduota S2.3 pav., (c). Šiame sprendime vienas M_{22} PMOP tranzistorius veikia tiesiniu režimu, o kitas tranzistorius $M_{22\mathrm{A}}$ kartu su srovę ribojančiu rezistoriumi R_{22} stabilizuoja V_{g2} bei įgyvendina $V_{\mathrm{g2}} - V_{\mathrm{GND}} > V_{\mathrm{DD}} - V_{\mathrm{g2}}$ sąlygą.



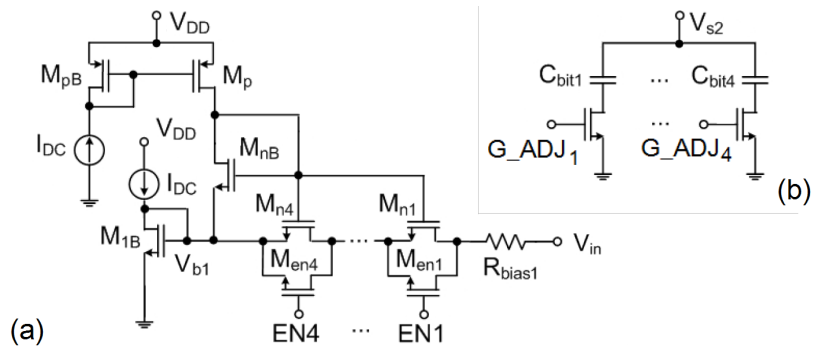
S2.3 pav. Varžinio pobūdžio grandinės, skirtos nustatyti V_{in} (a) ir V_{g2} (b) atraminiams priešįtampiams, bei naujai siūloma modifikuota PMOP tranzistorių pagrindu sukurta V_{g2} atraminio priešįtampio grandinė (c)



S2.4 pav. Diskretiškai valdomo stiprinimo talpinio grįžtamojo ryšio PVS struktūra

OTDR sistemoms yra būtinybė turėti PVS su valdomu stiprinimo koeficientu. Todėl šioje disertacijoje pasiūlyta diskretiškai valdomo stiprinimo talpinio grįžtamojo ryšio PVS struktūra, kuri pavaizduota S2.4 pav. Šioje struktūroje vienu metu valdomos įėjimo tranzistoriaus M_1 atraminių priešįtampių $R_{\mathrm{bias},1}$ (R_{SW}) ir grįžtamojo ryšio kondensatoriaus

C_1 (C_{SW}) masyvų grandinės. Šių masyvų grandinės atitinkamai pavaizduotos S2.5, (a) ir (b) paveiksluose. Kaip matyti iš S2.4 pav., C_2 kondensatoriaus talpa yra pastovi, o C_1 – diskretiškai keičiama žingsniu G_{ADJ}<1:4>, lygiagrečiai prijungiant atitinkamos talpos kondensatorius taip, kaip pavaizduota S2.5, (b) paveiksle. Toks C_1 talpos didinimas lemia ir diskretinį stiprinimo koeficiento keitimą aukštuosiuose dažniuose, priklausantį nuo C_1 ir C_2 kondensatorių santykio. Įėjimo tranzistoriaus M_1 atraminio priešįtampio grandinė (S2.5 pav. (a)) buvo modifikuota taip, kad diskretiniu žingsniu EN<1:4> būtų galima prijungti M_{n1}...M_{n4} tranzistorius, taip keičiant bendrą $R_{\mathrm{bias,1}}$ vertę ir valdant stiprinimą žemuosiuose dažniuose.



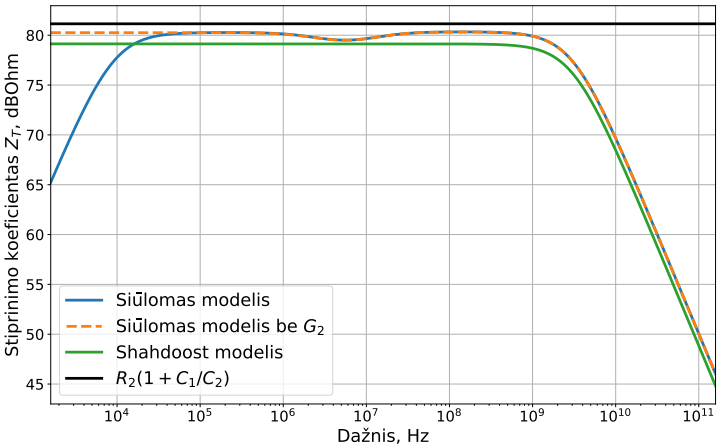
S2.5 pav. Diskretiškai valdomo stiprinimo koeficiento masyvų grandinės: (a) įėjimo tranzistoriaus M_1 atraminių priešįtampių grandinė, keičianti $R_{\mathrm{bias,1}}$; (b) valdomų kondensatorių grandinė, keičianti C_1

Stiprinimo koeficiento matematinė išraiška (S2.1) visiškai neatspinti realaus PVS grandinių stiprinimo koeficiento pobūdžio plačiame dažnių diapazone. Todėl šioje disertacijoje buvo pasiūlyta nauja matematinė išraiška, leidžianti tai įvertinti:

$$Z_{\mathrm{T}} = G_{\Sigma} Z_{\mathrm{in}} \approx \frac{G_1 G_2 G_3 G_{\mathrm{out}}}{1 + G_1 G_2 G_3 F_1} \cdot \frac{R_{\mathrm{bias,1}}}{1 + sR_{\mathrm{bias,1}} C_{\mathrm{T}}}. \tag{S2.2}$$

Šioje išraiškoje $s = \mathrm{j}\omega$, $R_{\mathrm{bias,1}}$ atitinka įėjimo tranzistoriaus M_1 atraminio priešįtampio rezistoriaus varžą, C_{T} – suminę fotodiodo C_{D} ir PVS įėjimo C_{IN} talpas, o G_{Σ} – sumines įtampos stiprinimo koeficientą. Pastarojoje išraiškoje G_1 atitinka įėjimo CS pakopos stiprinimą, G_2 – tarppakopinį aukštųjų dažnių filtro stiprinimą, G_3 – ištakos kartotuvo stiprinimą, G_{out} – ištakos kartotuvo stiprinimą po grįžtamojo ryšio ir F_1 – grįžtamojo ryšio stiprinimą. Literatūroje buvo bandymų matematiškai aprašyti talpinio grįžtamojo ryšio PVS stiprinimo koeficientą (Shahdoost et al., 2016). Tačiau analizės ir tyrimų metu pastebėta, kad šie matematiniai modeliai labiau atitinka idealias sąlygas ir mažiau tikslūs žemuosiuose dažniuose. S2.6 paveiksle pateikiami keturi matematiniai modeliai, aprašantys stiprinimo koeficiento dažnines charakteristikas: teorinė aproksimacija $R_2\,(1 + C_1/C_2)$, literatūroje aprašomas *Shahdoost* modelis bei disertacijoje siūlomas matematinis modelis su G_2 įvertinimu ir be jo. Neatitikimas tarp disertacijoje siūlomo ir *Shahdoost* modelio yra dėl to, kad pastarasis modelis atraminio priešįtampio grandines, srovės šaltinius laiko idealiais bei neįvertina G_2 stiprinimo koeficiento. Šio disertacijoje siūlomo modelio tei-

singumu buvo įsitikinta palyginus jį su kompiuterinio modeliavimo rezultatais, atliktais profesionaliu integrinių grandynų projektavimo *Cadence Virtuoso* programų paketu.



S2.6 pav. Talpinio grįžtamojo ryšio PVS Z_T modelių palyginimas

Šioje disertacijoje siūlomas ir išplėstinis srovės triukšmo energetinio spektro tankio dažninės charakteristikos matematinis modelis:

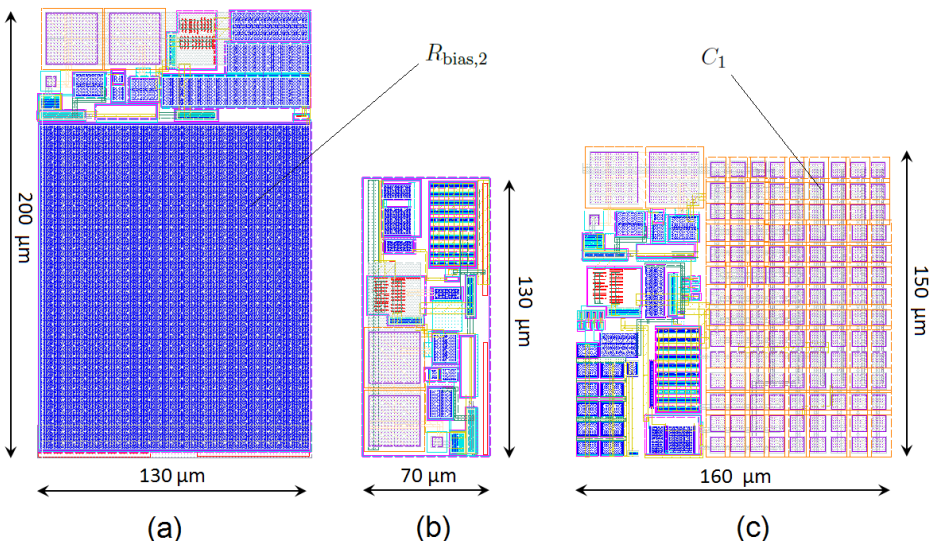
$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4\mathrm{k_B}T}{R_{\mathrm{bias},1}} + \frac{4\mathrm{k_B}TR_2}{Z_\mathrm{T}^2} + \frac{1}{Z_{\mathrm{in,eff}}^2}\left(\frac{8}{3}\frac{\mathrm{k_B}T}{g_{\mathrm{m},1}} + \frac{K_{\mathrm{f,M1}}}{f}\frac{1}{C_{\mathrm{ox}}W_{M1}L_{\mathrm{M1}}}\right) + G_{\mathrm{M5}}^2\frac{K_{\mathrm{f,M5}}}{f}\frac{1}{C_{\mathrm{ox}}W_{\mathrm{M5}}L_{\mathrm{M5}}}. \tag{S2.3}$$

Šioje išraiškoje: $\mathrm{k_B}$ – Boltzmano konstanta, T – temperatūra, $Z_{\mathrm{in,eff}}$ – efektyvioji įėjimo pilnutinė varža (impedansas), $g_{\mathrm{m,X}}$ – M_X tranzistoriaus statumas, $K_{\mathrm{f,MX}}$ – M_X tranzistoriaus pereigos laidis, f – dažnis, C_{ox} – užtūros oksido savitoji talpa, W_{MX} ir L_{MX} – atitinkamai M_X tranzistoriaus kanalo plotis bei ilgis, G_{M5} – M_5 tranzistoriaus mirgėjimo triukšmo stiprinimas. Ši matematinė išraiška turi keturias pagrindines dedamąsias. Pirmoji dedamoji apibūdina $R_{\mathrm{bias},1}$ rezistoriaus terminį triukšmą, antroji dedamoji – R_2 rezistoriaus sukeliamą terminį triukšmą, priklausantį nuo Z_T, trečioji dedamoji aprašo įėjimo tranzistoriaus M_1 terminius kanalo ir $1/f$ (mirgėjimo) triukšmus, o ketvirtoji – M_5 tranzistoriaus $1/f$ triukšmus. Kaip matyti iš disertacijoje pasiūlytos išraiškos, žemuosiuose dažniuose triukšmo mažėjimą lemia $1/f$ triukšmai, terminiai triukšmai turi baltojo triukšmo pobūdį ir nepriklauso nuo dažnio bei nulemia minimalų triukšmo lygį vidutiniuose dažniuose, o trečioji triukšmo dedamoji lemia triukšmo charakteristiką aukštuosiuose dažniuose, t. y. triukšmų didėjimą didėjant dažniui, nes $Z_{\mathrm{in,eff}}$ yra nuo dažnio mažėjantis dydis. (Keshri, 2010) darbe taip pat pateikiamas srovės triukšmo spektrinio tankio matematinis modelis, tačiau jis tinkamas tik idealiems atvejams ir mažiau tikslus žemuosiuose ir vidutiniuose dažniuose. Kaip ir stiprinimo koeficiento atveju, šis siūlomas matematinis modelis buvo palygintas su kompiuterinio modeliavimo rezultatais, atliktais *Cadence Virtuoso* programų paketu.

3. Talpinio grįžtamojo ryšio PVS projektavimas ir tyrimas

Remiantis antrajame skyriuje pasiūlyta talpinio grįžtamojo ryšio PVS architektūra ir matematiniais modeliais, suprojektuotos ir ištirtos kelios šios architektūros versijos, taikant submikronines 0,18 µm KMOP ir 0,25 µm BiKMOP gamybos technologijas bei profesionalų integrinių grandynų projektavimo *Cadence Virtuoso* programų paketą.

S3.1 pav. pavaizduotos trys skirtingos suprojektuoto talpinio grįžtamojo ryšio PVS topologijų versijos, naudojant TSMC 0,18 µm KMOP gamybos technologiją. S3.1 pav., (a), pavaizduotas fiksuoto Z_{T}=10 kΩ stiprinimo sprendimas su visiškai varžinėmis V_{in} ir V_{g2} atraminio priešįtampio grandinėmis (plotas luste yra apie (200×130) µm^2). Pritaikius disertacijoje pasiūlytą PMOP tranzistorių pagrindu sukurtą V_{g2} atraminio priešįtampio grandinę, užimamą plotą luste pavyko sumažinti net iki (130×70) µm^2 (S3.1 pav., (b)). Galiausiai, įgyvendinus diskretiškai 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ žingsniu valdomo stiprinimo PVS architektūrą kartu su PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandine, pavyko suprojektuoti (150×160) µm^2 užimamo ploto luste topologiją (S3.1 pav., (c)).

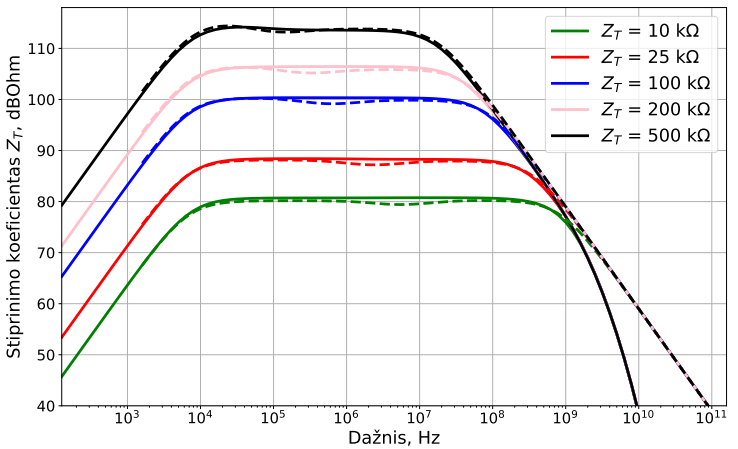


S3.1 pav. Trys skirtingos suprojektuoto talpinio grįžtamojo ryšio PVS topologijų versijos, naudojant TSMC 0,18 µm KMOP gamybos technologiją: (a) fiksuoto 10 kΩ stiprinimo su visiškai varžine atraminio priešįtampio grandine; (b) fiksuoto 10 kΩ stiprinimo su PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandine; (c) diskretiškai žingsniu valdomo stiprinimo, kartu su PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandine

S3.1 pav., (c), pavaizduotoje topologijoje C_1 kondensatoriaus masyvo įgyvendinimas didelėms stiprinimo vertėms užima apie 50 % viso ploto. Konfigūracijos su didžiausiu stiprinimo koeficientu (Z_{T} = 200 kΩ ir 500 kΩ) yra reikliausios užimamam plotui luste,

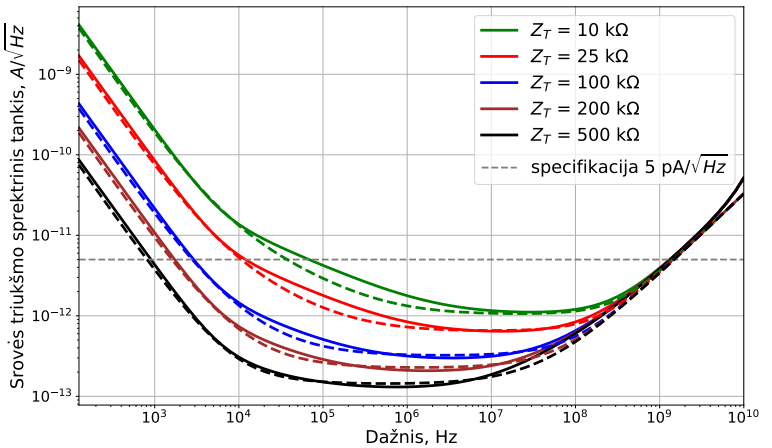
nes būtina įgyvendinti net 120 pF siekiančią C_1 talpą. Gauti rezultatai patvirtina, kad siūloma talpinio grįžtamojo ryšio PVS architektūra su diskretiškai valdomu stiprinimu nėra sudėtinga, nes C_1 ir $R_{\mathrm{bias},1}$ reikšmės tiesiog tiesiškai didinamos, atsižvelgiant į reikiamą / siekiamą gauti stiprinimo koeficientą Z_{T}. Visų šių konfigūracijų vartojamoji galia išlieka praktiškai vienoda ir artima 21 mW, kai naudojama 1,8 V maitinimo įtampa. Likę grandinės parametrai išlieka vienodi visoms stiprinimo konfigūracijoms.

Pagrindiniai siūlomos architektūros PVS parametrai buvo gauti kompiuteriniu būdu modeliuojant suprojektuotas topologijas. Stiprinimo koeficiento priklausomybė nuo dažnio pavaizduota S3.2 paveiksle. Šiame paveiksle matyti penki diskretiškai valdomo stiprinimo žingsniai. Esant stiprinimo koeficientui Z_{T} = 10 kΩ, pasiekiamas didžiausias 1,0 GHz praleidžiamųjų dažnių juostos plotis. O esant Z_{T} = 500 kΩ, praleidžiamųjų dažnių juostos plotis sumažėja iki 0,03 GHz. Siūlomo stiprinimo koeficiento matematinio modelio neatitikimas lyginant su *Cadence* modeliavimo rezultatais visais pateiktais atvejais neviršija 5 %, matuojant šį neatitikimą dažnių diapazone iki 1,0 GHz. Gautas neatitikimas rodo siūlomo stiprinimo koeficiento matematinio modelio teisingumą ir galimybes jį taikyti kuriant bei tobulinant valdomo stiprinimo talpinio grįžtamojo ryšio PVS.

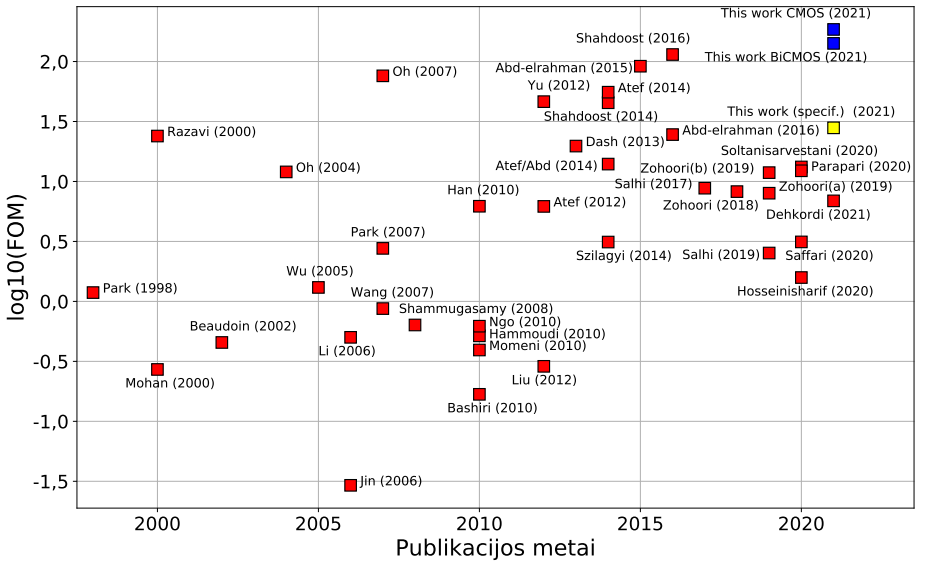


S3.2 pav. Stiprinimo koeficiento priklausomybė nuo dažnio, esant skirtingiems Z_{T}: ištisine linija rodomi *Cadence Virtuoso* modeliavimo rezultatai, o punktyrinėmis linijomis siūlomo matematinio modelio

Srovės triukšmo spektrinio tankio priklausomybė nuo dažnio yra pavaizduota S3.3 paveiksle. Srovės triukšmo spektrinio tankio reikšmė prie 500 MHz ir Z_{T} = 10 kΩ yra apie 1,8 pA/$\sqrt{\mathrm{Hz}}$ KMOP atveju (BiKMOP atveju apie 1,6 pA/$\sqrt{\mathrm{Hz}}$). Siūlomas matematinis modelis turi apie 15 % neatitikimą esant 500 MHz dažniui ir Z_{T} = 10 kΩ, lyginant su kompiuterinio modeliavimo rezultatais, bei puikiai tinkamas matematinei triukšmo komponenčių analizei ir galimoms mažinimo kryptims nustatyti. Pasiūlytas PVS buvo įgyvendintas ir IHP 0,25 µm BiKMOP gamybos technologijoje. Suprojektuotos topologijos plotas pasiektas (200×180) µm^2 (50 % didesnis, lyginant su TSMC 0,18 µm KMOP). Kiti geriausi pasiekti rezultatai yra šie: 900 MHz praleidžiamųjų dažnių juosta, net 1,6 pA/$\sqrt{\mathrm{Hz}}$ srovės triukšmo spektrinis tankis, esant 29 mW vartojamajai galiai ir 2,5 V maitinimo įtampai.



S3.3 pav. Srovės triukšmo spektrinio tankio priklausomybė nuo dažnio, esant skirtingiems Z_{T}: ištisine linija rodomi *Cadence Virtuoso* modeliavimo rezultatai, o punktyrinėmis linijomis siūlomo matematinio modelio



S3.4 pav. Disertacijoje gautos kokybės funkcijos reikšmės palyginimas su kitų autorių darbais esant skirtingiems publikavimo metams. Melsvi taškai atitinka suprojektuotų rezultatų kokybės funkcijos reikšmes (KMOP ir BiKMOP), o gelsvas – išsikeltų ir siektinų pagrindinių PVS parametrų rinkinio

Disertacijoje siūlomo talpinio grįžtamojo ryšio PVS, suprojektuoto taikant submikroninę TSMC 0,18 µm KMOP gamybos technologiją ir esant Z_{T} = 10 kΩ vertei, kokybės funkcijos reikšmė yra 185. Šios vertės palyginimas su kitų autorių darbais esant skirtin-

giems publikavimo metams pavaizduotas S3.4 pav. Naudojant IHP 0,25 µm BiKMOP gamybos technologiją, pasiekta reikšmė yra apie 141. Disertacijoje pasiūlyto talpinio grįžtamojo ryšio PVS kokybės funkcijos, reikšmė yra didesnė už geriausių (Abd-elrahman et al., 2015; Shahdoost et al., 2016) darbų įverčius.

Bendrosios išvados

1. Taikant naujai sudarytą kokybės funkciją, atlikta palyginamoji PVS analizė parodė, kad talpinio grįžtamojo ryšio PVS architektūra, kurios kokybės funkcijos reikšmė gali siekti daugiau nei 114, yra tinkamiausia kuriant valdomo stiprinimo, plačiajuosčius, mažatriukšmius PVS, įgyvendinant juos viename luste šiuolaikinėmis submikroninėmis KMOP ir BiKMOP gamybos technologijomis.
2. Sukurta originali PVS architektūra su diskrečiai valdomo grįžtamojo ryšio kondensatorių ir atraminio priešįtampio grandinių masyvais, leidžiančiais įgyvendinti diskretiškai valdomą stiprinimą, ypač plačią praleidžiamųjų dažnių juostą ir mažus triukšmus. Taip pat šioje architektūroje pasiūlyta originali PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandinė, leidžianti pakeisti visiškai varžinio pobūdžio grandinę ir taip itin sumažinti užimamą plotą luste.
3. Pasiūlyti stiprinimo koeficiento ir srovės triukšmo spektrinio tankio matematiniai modeliai, leidžiantys apskaičiuoti ir praplėsti šių parametrų tikslumą dažnių ruože iki 1 GHz. Stiprinimo koeficiento matematiniame modelyje išskiriamos ir apskaičiuojamos pagrindinės schemotechninės dalys, veikiančios šio modelio tikslumą, o triukšmų matematiniame modelyje išskiriami pagrindiniai triukšmų šaltiniai, turintys didžiausią įtaką suminiam srovės triukšmo spektriniam tankiui. Tyrimų metu įsitikinta, kad šių matematinių modelių neatitiktis kompiuterinių modeliavimų metu gautiems rezultatams yra: 5 % stiprinimo koeficientui, matuojant šią neatitiktį dažnių juostoje iki 1 GHz; 15 % srovės triukšmo spektriniam tankiui, esant 500 MHz dažniui ir 10 kΩ stiprinimo koeficientui.
4. Taikant submikroninę TSMC 0,18 µm KMOP integrinių grandynų gamybos technologiją, suprojektuotas ir ištirtas talpinio grįžtamojo ryšio PVS, užtikrinantis 1 GHz praleidžiamųjų dažnių juostą, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ diskretiniu žingsniu valdomą stiprinimą, 1,8 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinį tankį, esant 21 mW vartojamajai galiai ir 1,8 V maitinimo įtampai, bei užimantis (150×160) µm^2 plotą luste ir pasiekiantis kokybės funkcijos reikšmę 185. Šioje architektūroje panaudota originali PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandinė leido užimamą plotą luste sumažinti net 65 %, lyginant su visiškai varžine atraminio priešįtampio grandine.
5. Taikant submikroninę IHP 0,25 µm BiKMOP integrinių grandynų gamybos technologiją suprojektuotas ir ištirtas talpinio grįžtamojo ryšio PVS su PMOP tranzistorių pagrindu sukurta atraminio priešįtampio grandine, užtikrinantis 900 MHz praleidžiamųjų dažnių juostą, 10 kΩ, 25 kΩ, 100 kΩ, 200 kΩ ir 500 kΩ diskretiniu žingsniu valdomą stiprinimą, net 1,6 pA/$\sqrt{\text{Hz}}$ srovės triukšmo spektrinį tankį, esant 29 mW vartojamajai galiai ir 2,5 V maitinimo įtampai, bei užimantis (200×180) µm^2 plotą luste ir pasiekiantis kokybės funkcijos reikšmę 141.

Annexes[1]

Annex A. Declaration of Academic Integrity

Annex B. The Copies of Scientific Publications by the Author on the Topic of the Dissertation

[1]The annexes are supplied in the enclosed compact disc.

Agata ROMANOVA

DESIGN OF TRANSIMPEDANCE AMPLIFIERS
FOR BROADBAND TIME-DOMAIN OPTICAL
REFLECTOMETER SYSTEMS

Doctoral Dissertation

Technological Sciences,
Electrical and Electronic Engineering (T 001)

PLAČIAJUOSČIŲ LAIKO SRITIES OPTINIŲ
REFLEKTOMETRINIŲ SISTEMŲ PEREINAMOSIOS
VARŽOS STIPRINTUVŲ KŪRIMAS

Daktaro disertacija

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elektros ir elektronikos inžinerija (T 001)

Anglų kalbos redaktorė Rasa Akstinienė
Lietuvių kalbos redaktorė Dalia Markevičiūtė
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Spausdino UAB „Ciklonas“,
Žirmūnų g. 68, LT-09124 Vilnius