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MID-BAND 5G WIRELESS NETWORK POWER AMPLIFIER RESEARCH

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Abstract

This dissertation addresses the problems of ensuring efficient radio frequency transmission for 5G wireless networks. Taking into account, that the next generation 5G wireless network structure will be heterogeneous, the device density and their mobility will increase and massive MIMO connectivity capability will be widespread, the main investigated problem is formulated – increasing the efficiency of portable mid-band 5G wireless network CMOS power amplifier with impedance matching networks.

The dissertation consists of four parts including the introduction, 3 chapters, conclusions, references and 3 annexes.

The investigated problem, importance and purpose of the thesis, the object of the research methodology, as well as the scientific novelty are defined in the introduction. Practical significance of the obtained results, defended statements and the structure of the dissertation are also included.

The first chapter presents an extensive literature analysis. Latest advances in the structure of the modern wireless network and the importance of the power amplifier in the radio frequency transmission chain are described in detail. The latter is followed by different power amplifier architectures, parameters and their improvement techniques. Reported impedance matching network design methods are also discussed. Chapter 1 is concluded distinguishing the possible research vectors and defining the problems raised in this dissertation.

The second chapter is focused around improving the accuracy of designing lumped impedance matching network. The proposed methodology of estimating lumped inductor and capacitor parasitic parameters is discussed in detail providing complete mathematical expressions, including a summary and conclusions.

The third chapter presents simulation results for the designed radio frequency power amplifiers. Two variations of Doherty power amplifier architectures are presented in the second part, covering the full step-by-step design and simulation process. The latter chapter is concluded by comparing simulation and measurement results for all designed radio frequency power amplifiers.

General conclusions are followed by an extensive list of references and a list of 5 publications by the author on the topic of the dissertation.

5 papers, focusing on the subject of the discussed dissertation, have been published: three papers are included in the *Clarivate Analytics Web of Science* database with a citation index, one paper is included in *Clarivate Analytics Web of Science* database *Conference Proceedings*, and one paper has been published in unreferred international conference preceedings. The author has also made 9 presentations at 9 scientific conferences at a national and international level.

Reziumė

Disertacijoje nagrinėjamos 5G belaidžio ryšio sistemų efektyvumo didinimo problemos. Įvertinant tai, kad naujos kartos 5G belaidžio ryšio įranga bus įvairialytė bei mobili, numatomos daugiakanalio ryšio galimybės ir ženkliai išaugęs šios įrangos tankis, suformuluojama pagrindinė disertacijoje sprendžiama problema – nešiojamų vidutinių dažnių 5G belaidžio ryšio įrenginių KMOP galios stiprintuvo su suderinimo grandynais veikimo efektyvumo didinimas.

Disertaciją sudaro įvadas, trys skyriai, bendrosios išvados, naudotos literatūros ir autoriaus publikacijų disertacijos tema sąrašai bei trys priedai.

Įvadiniame skyriuje aptariama tiriamoji problema, darbo aktualumas, aprašomas tyrimų objektas, formuluojami darbo tikslai bei uždaviniai, aprašoma tyrimų metodika, darbo mokslinis naujumas, darbo rezultatų praktinė reikšmė, ginamieji teiginiai bei disertacijos struktūra.

Pirmame skyriuje pateikiama išsami literatūros analizė, aprašomos naujausios belaidžio ryšio tinklų struktūros bei jų ypatumai, išskiriant galios stiprintuvo svarbą siųstuvo grandyne. Toliau pateikiama belaidžio ryšio galios stiprintuvų architektūrų bei pagrindinių parametrų analizė, literatūroje aptinkami impedansų suderinimo grandynų projektavimo metodai. Pirmasis skyrius užbaigiamas išskiriant pagrindines belaidžio ryšio galios stiprintuvų ir impedansų suderinimo grandynų projektavimo ir tyrimo kryptis.

Antrajame skyriuje analizuojamos impedansų suderinimo grandynų projektavimo metodikų tobulinimo kryptys. Išsamiai aprašoma pasiūlyta impedansų suderinimo grandynų, taikant sutelktųjų parametrų komponentus, metodika ir algoritmas, pateikiant ir paaiškinant panaudotas matematines išraiškas.

Trečiame skyriuje pateikiami suprojektuotų ir ištirtų galios stiprintuvų modeliavimo, eksperimentinių matavimų bei tyrimų rezultatai. Pateikiamos ir išsamiai aprašomos dvi Doherty architektūros galios stiprintuvų konfigūracijos. Pastarasis skyrius užbaigiamas visų suprojektuotų galios stiprintuvų modeliavimo ir eksperimentinių matavimo rezultatų palyginimu.

Šios disertacijos tyrimus apibendrina bendrosios išvados ir pateikiamas išsamus literatūros sąrašas bei penkių autoriaus publikacijų sąrašas disertacijos tema.

Disertacijos tema paskelbtos trys publikacijos moksliniuose žurnaluose, referuojamuose *Clarivate Analytics Web of Science* duomenų bazėje, ir turinčiuose citavimo rodiklius, bei dvi publikacijos – konferencijų straipsnių rinkiniuose, iš kurių viena priskiriama *Clarivate Analytics Web of Science* duomenų bazės *Conference Proceedings* leidiniams, o antroji nereferuojamoje tarptautinės užsienio konferencijos medžiagoje. Disertacijos rezultatai buvo pristatyti devyniose konferencijose Lietuvoje ir užsienyje.

Notations

Symbols

A_v – amplifier gain;

C – capacitance;

f – frequency;

G – conductance;

I – current;

K_f – amplifier stability factor;

L – inductance;

L_x – transistor channel length;

n – traveling wave amplifier stage count;

P – power;

Q – quality factor;

R – resistance;

S_{11}, S_{12}, S_{21}, S_{22} – scattering parameters: input port voltage reflection coefficient, reverse voltage gain (isolation), forward voltage gain, output port voltage reflection coefficient;

t – time;

U – voltage;
V_{bias} – bias voltage;
V_{DD} – supply voltage;
W_x – transistor width;
X, X_L, X_C – reactive, reactive inductive and reactive capacitive impedance;
Z – complex impedance;
Z_0 – transmission line characteristic impedance;
$\Gamma(\omega)$ – reflection coefficient as a function of angular frequency;
η – efficiency;
θ – conduction angle;
λ – wavelength;
τ – time constant;
ω – angular frequency.

Abbreviations

ACLR – adjacent channel leakage ratio;
ADC – analog-to-digital converter;
AM/PM – amplitude/phase modulation;
ASIC – application specific integrated circuit;
BJT – bipolar junction transistor;
BW – bandwidth;
CCA – current conduction angle;
CG – common gate;
CMOS – complementary metal–oxide semiconductor;
CP – cell planning;
CW – continuous wave signal, sine wave;
DAC – digital-to-analog converter;
DC – direct current;
DPA – Doherty power amplifier;
DPD – digital predistortion;
DSP – digital signal processor;
EER – envelope elimination and restoration;
ESR – equivalent series resistance;
ET – envelope tracking;
EVM – error vector magnitude;
FPGA – field programmable gate array;

GUI – graphical user interface;
HB – harmonic balance;
IC – integrated circuit;
IF – intermediate frequency;
IMn – *n*-th order intermodulation product;
IMNS – impedance matching network synthesis;
IoT – Internet of Things;
I/Q – in-phase quadrature modulated signal;
LDO – low dropout regulator;
LNA – low noise amplifier;
LPF – low pass filter;
LTE – Long-Term Evolution;
MCU – microcontroller unit;
MIMO – multiple-input multiple-output;
MMIC – monolithic microwave integrated circuit;
MOSFET – metal oxide field effect transistor;
M2M – machine to machine;
NF – noise figure;
NMOS – *n*-type metal-oxide semiconductor transistor;
OFDM – orthogonal frequency-division multiplexing;
PA – power amplifier;
PAE – power added efficiency;
PCB – printed circuit board;
PMOS – *p*-type metal-oxide semiconductor transistor;
PSRR – power source rejection ratio;
P1dB, IR-P1dB, OR-P1dB – (input-, output-referred) amplifier 1 dB compression point;
RF – radio frequency;
SDR – software defined radio;
SAW – surface acoustic wave;
SP – small-signal parameter simulation;
SPDT – single-pole dual-throw;
SRF – self-resonant frequencies;
TLine – transmission line;
TT, SS, FF corner – typical, slow and fast corner simulation conditions;
TWA – traveling wave amplifier;
VSWR – voltage standing wave ratio.

Contents

[1] The annexes are supplied in the attached compact disc.

Introduction

Problem Formulation

In recent years, the shift from the mature 4G to the developing 5G wireless communications has created new challenges and opportunities for high-frequency and millimeter-wave circuits and components. Overall, 5G systems will impose stringent power, efficiency and linearity on power amplifiers (PA): 24 dBm maximum portable device output power, increasing the efficiency to reach the largest achievable theoretical 50% mark for linear power amplifier and increasing the operating bandwidth (Pham et al., 2017).

It is widely known that the RF PA is the most power-hungry component in radio transmitters and transceivers, thus its performance directly affects the efficiency of the overall system. When modulated signals are amplified, the PA can operate anywhere up to 12 dB below its compression point, depending on the modulation scheme. In these conditions, the efficiency of the PA can be half of the efficiency at the compression point, leading to a smaller battery life for portable wireless devices. The next-generation 5G network is planned to connect multiple transceivers with massive MIMO capabilities, so the efficiency of the whole system becomes a priority. Although the *III-V* group semiconductors provide unprecedented achievable parameters for watt-level radio frequency PAs, the tendencies of shifting to an array of small- to medium-power milliwatt-level

heterogeneous wireless network elements open up more capabilities to the already widely used, low-cost and scalable CMOS process. Taking into account all of the above, there is a need for CMOS PA architectures, which comply with the specified 5G transmission power levels, reducing the quiescent current and operating in a wide frequency range.

The 5G spectrum is divided into three bands, including decimeter-, centimeter- and millimeter-wave frequencies. This results in low-, mid- and high-band 5G frequency range accordingly. 3GPP standard (European Standards Organization ETSI, 2018) divides the licensed bands into two groups, named FR1 (sub-6 GHz) and FR2 (above 24 GHz). The latter standard doesn't include unlicensed bands both in Europe (5.9–6.4 GHz) and the USA (5.9–7.1 GHz), which could also be included in the FR1 range, as they serve the main purpose of broadband radio service. Therefore, the named mid-band 5G frequency range (Qualcomm Technologies Inc., 2017) spans from 1 GHz to 7.1 GHz and is intended to be used for local high-speed data rate coverage, so their deployment has the highest priority. Other 5G bands are low-band 5G, spanning up to 1 GHz and the high-band 5G, which includes frequencies above 24 GHz. As a result, the PA architecture should operate efficiency at different input signal power levels and be applicable in all 5G bands without linearization restrictions.

A common problem, which arises when researching and designing PAs is related with matching a source impedance to a load. Impedance matching networks are usually placed off-chip due to the large occupied area, reducing increased integrated circuit fabrication cost. The off-chip impedance matching network usually contain lumped components with innate parasitic parameters, which affect the matching response S_{11}. If the latter parasitic parameters are neglected, multiple calculation and measurement iterations are required to match the source to a load under given conditions. This can lead to increased research and design costs. Methods, which include lumped component parasitic parameters that affect the matching response shift in the frequency domain, have not been proposed. As a result, new methods and software tools, capable of calculating PA impedance matching networks with lumped component parasitic parameters, are required.

Taking into account, that the next generation 5G wireless network structure will be heterogeneous, the device with MIMO connectivity capability density will increase, the main investigated problem is formulated – increasing the efficiency of portable mid-band 5G wireless network CMOS power amplifier with impedance matching networks. In order to solve the formulated problem, a hypothesis is raised and proven: Doherty architecture power amplifiers with impedance matching networks, designed in deep submicron CMOS processes, can provide an increased power added efficiency in a wide range of input signal power and is suitable to be implemented in 5G wireless systems.

Relevance of the Thesis

The structure of the modern wireless network rapidly evolves and the maturing 4G networks pave the way to next-generation 5G communication. 5G specifications, compared to that of 4G networks, includes user experienced data rates in the region of 100 Mbit/s to 1 Gbit/s; connection density of 1 million connections per km^2; end-to-end latency in the millisecond level; intermediate frequency bandwidths of up to 150 MHz; and mobility up to 500 km/h (Qualcomm Technologies Inc., 2017; The European Conference of Postal and Telecommunications Administrations CEPT, 2018,). Next-generation 5G communication can be the bind Internet of Things (IoT) and Internet of Vehicles (IoV) to form the Internet of Everything (IoE). Therefore, the 5G wireless technologies can accelerate Industry 4.0. Heterogeneous 5G wireless networks also include communication with multiple portable battery-powered low-power sensors, which require efficient transceivers. Taking into account, that the power amplifier is one of the main blocks in the transmission chain, which defines its efficiency, research in the area of power amplifier architectures and their impedance matching networks is required (Rao & Prasad, 2018). Due to the announced tendencies of shifting to an array of small- to medium-power heterogeneous wireless network elements (including different architecture PAs), the number of published scientific publications covering the latter field, based on mature submicron CMOS processes, is rapidly increasing. Different classical and advanced PA architectures with various modifications are currently proposed, but it is unclear which architecture is most suitable for the next generation portable wireless network devices. The CMOS process is typically the process of choice when a both high levels of integration and functionality are required. Therefore, other radio frequency components can readily be integrated alongside with the power amplifier in a single CMOS chip (Zampardi, 2010). This tendency can be also seen from the leading radio frequency transceiver manufacturers (Analog Devices, 2019; Lime Microsystems, 2019; Texas Instruments, 2019). Therefore, research in the field of CMOS radio frequency power amplifiers for 5G wireless networks, aiming for the highest obtainable efficiency at the smallest price and occupied area, may help to drive the advances in the field.

Research in the field of radio frequency transceiver blocks is not widespread in Lithuania. Papers covering the latter topic have been published by VGTU researchers M. Jurgo (Jurgo et al., 2019), V. Mačaitis (Mačaitis et al., 2019), K. Kiela (Kiela, et al., 2016), J. Charlamov (Charlamov et al., 2010), as well as VU researcher P. Sakalas (Sakalas et al., 2008). Companies UAB "Lime Microsystems" and UAB "Si Femto" located in Vilnius and Kaunas accordingly are working in the field of radio frequency and high-speed application specific integrated circuit design.

Summarizing all of the above, the field of next-generation 5G wireless network power amplifiers and their impedance matching networks is not sufficiently investigated and described, the research conducted in this thesis are relevant, and the obtained results alongside with further research will accelerate the development of the next generation 5G wireless networks.

The Object of Research

The object of research – radio frequency power amplifier architectures with impedance matching networks suitable for mid-band 5G wireless networks.

The Aim of the Thesis

The aim of the thesis is to define and investigate the most promising advanced radio frequency power amplifier architectures with impedance matching networks for mid-band 5G wireless networks.

Tasks of the Thesis

In order to achieve the aim, the following problems had to be solved:

1. Conduct extensive research on different radio frequency power amplifier architectures, providing qualitative and quantitative analysis results.
2. Design and conduct experimental research with different architecture radio frequency power amplifiers for mid-band 5G wireless networks.
3. Conduct extensive research on the existing methods of designing power amplifier impedance matching networks and propose a novel lumped component impedance matching network calculation algorithm and mathematical model, which includes parasitic component parameters.

Research Methodology

Analytical, mathematical, computer simulation and experimental research methods have been chosen in order to investigate the radio frequency power amplifier architectures and their impedance matching networks. Analytical method has been applied during the review of different radio frequency power

amplifier architectures and impedance matching network design approaches. Mathematical, computer simulation and experimental methods have been applied during the research of different wireless power amplifier architectures have and impedance matching networks. *TSMC* 0.18 μm and *IBM (GlobalFoundries)* 0.13 μm CMOS processes have been used designing classical, traveling wave and Doherty power amplifiers. All designed radio frequency power amplifiers have been simulated using a professional integrated circuit design platform *Cadence Virtuoso*. The proposed impedance matching network synthesis (*IMNS*) toolbox has been created using *SKILL* programming language within the *Cadence Virtuoso* design platform. The printed circuit boards used for both power amplifier and impedance matching network research have been designed using *Altium Designer*. The power amplifiers and impedance matching networks were investigated in the 0.1–7.1 GHz frequency domain, which is included in the mid-band 5G range.

Scientific Novelty of the Thesis

The following significant results for electrical and electronics engineering science have been obtained during the preparation of this dissertation:

1. A qualitative and quantitative approach of characterizing state of the art advanced power amplifier architectures, defining their advantages and disadvantages in deep submicron (0.35–0.11 μm) CMOS nodes and their adaptability when designing 5G wireless transmitters and transceivers for different 5G bands, has been proposed.
2. A modification of the Doherty power amplifier architecture with a simplified impedance inverter has been proposed, leading to a 12% occupied area reduction in deep submicron (0.35–0.11 μm) CMOS nodes and maintaining the *PAE* value at 3 dB back-off close to that of a saturated DPA.
3. A novel lumped component impedance matching network synthesis algorithm and mathematical model, which takes into account different size lumped component parasitic parameters, their dielectric properties and operating frequency, has been proposed.

Practical Value of the Research Findings

A qualitative and quantitative assessment, which includes different advanced power amplifier architecture implemented in various manufacturing processes,

has been proposed and can be used during the design of low-, mid- and high-band 5G wireless systems. The power amplifier architectures, which were investigated in this dissertation have been designed and fabricated using *TSMC* 0.18 μm and *IBM (GlobalFoundries)* 0.13 μm deep submicron CMOS processes. The proposed DPA architecture modification can be implemented in mid-band 5G wireless transmitter and transceiver design and research phase. The proposed novel impedance matching network synthesis algorithm and mathematical model, as well as the software plug-in based on the latter model and algorithm, can reduce the time and cost of designing impedance matching networks for the next generation 5G power amplifiers. The latter plug-in is integrated into the professional integrated circuit design platform *Cadence Virtuoso*, therefore can be used for engineering and research purposes.

The research results presented in this dissertation have been used implementing the following projects and scientific works:

- "Smart RFID card Design" (No. 11796, 2014–2015) project.
- "Design and research on high frequency integrated circuits for smart wireless communication systems" (No. 10124, 2014–2015) research work.
- "Printed circuit board for a software-defined radio, based on a multistandard transceiver, design" (No. 15222, 2016–2017) project.
- "Radio frequency power amplifier architecture research for 4G and future 5G wireless networks" (No. 09.3.3-LMT-K-712-03-0007, 2017–2018) research work.
- "Design and Research of Internet of Things (IoT) Framework Model and Tools for Intelligent Transport Systems" (No. 01.2.2-LMT-K-718-01-0054, 2017–2019) research work.
- "A modern small-scale high data throughput armored lock surveillance system design" (No. 17582, 2017–2018) project.

The Defended Statements

1. The classical linear and traveling wave PA architectures, implemented in *IBM (GlobalFoundries)* 0.13 μm deep submicron CMOS process, are not suitable for mid-band 5G wireless transmitters and transceivers due the peak 25% *PAE* at different input signal powers for both architectures and restrictions in the matched bandwidth (up to 400 MHz) for classical PAs.
2. Doherty architecture PA implemented deep submicron *TSMC* 0.18 μm CMOS process can provide a *PAE* in the range from 25% to the maximum

theoretical 50% for linear PAs at a 3 dB back-off power and a center frequency of 6.5 GHz.

3. Taking into account surface mount lumped component parasitic parameters when impedance matching networks are calculated, the simulation and measurement iteration count can be reduced to 1–3 in the low- and mid-band 5G frequency ranges.
4. In order to match a source to load using lumped inductors and capacitors, only the most sensitive to change lumped surface-mount component in the impedance matching network needs to be high precision (less than or equal to 5%) while all other component tolerances increased according to the IEC/EN 60062 standard.

Approval of the Research Findings

Five papers have been published in journals based on or related to the results presented in this dissertation. Four of the published five papers are included in the *Clarivate Analytics Web of Science* database. Papers (Vasjanov & Barzdenas 2018, Oct.) and (Vasjanov & Barzdenas 2018, Sep.) have been published in a second quartile (Q2) journal with an impact factor 2.11 (2017). Paper (Vasjanov & Barzdenas 2016) has been published in a fourth quartile (Q4) journal with an impact factor of 0.476 (2017). Paper (Vasjanov & Barzdenas 2017) has been published in conference proceedings, which are included in the *Clarivate Analytics Web of Science* database. Paper (Vasjanov & Barzdenas 2018, May) has been published in unreferred international conference "*CDNLive EMEA 2018*" proceedings.

The author has made 9 presentations at 9 scientific conferences in Lithuania and abroad:

- Cadence User Conference "*CDNLive EMEA 2018*". Munchen, Germany, 7–9 May 2018.
- 2nd IEEE International Open Conference "*2018 Electrical, Electronic and Information Sciences (eStream 2018)*". Vilnius, Lithuania, 26 April 2018.
- 21st Conference for Young Researchers "*Science – future of Lithuania*". Vilnius, Lithuania, 16 March 2018.
- 18th Lithuania-Belarus IEEE Workshop "*Advanced microwave devices and systems*". Vilnius, Lithuania, 8–9 December 2017.
- University of Rochester (USA) seminar. Rochester, USA, 9 May 2017.
- 1st IEEE International Open Conference "*2017 Electrical, Electronic and Information Sciences (eStream 2017)*". Vilnius, Lithuania, 27 April 2016.

- National conference "*2016 Electrical, Electronic and Information Sciences (eStream 2016)*". Vilnius, Lithuania, 19 April 2016.
- 19th Conference for Young Researchers "*Science – future of Lithuania*". Vilnius, Lithuania, 18 March 2016.
- 16th Lithuania-Belarus IEEE Workshop "*Advanced microwave devices and systems*". Vilnius, Lithuania, 4 December 2015.

Structure of the Dissertation

The dissertation is structured around three chapters, general conclusions and an extensive list of references and a list of 5 publications by the author on the topic of the dissertation.

The volume of the dissertation is 151 pages, excluding annexes. The text contains 70 numbered formulas, 59 figures and 21 tables.

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1

Modern Radio Frequency Power Amplifier Review and Analysis

The following chapter presents a review of modern state of the art radio frequency (RF) power amplifiers (PA), published in scientific journals. The analysis of PA fundamental metrics as well as their improvement techniques and circuits is followed by different amplifier architectures, which are characterized and parametrized, highlighting the main advantages and disadvantages. Impedance matching is a concurrent part of the PA design process, hence existing methods are also discussed. The topics analyzed in this section define the contemporary RF PA evolution vectors, denoting the directions of further improvement. Chapter 1 concludes with formulating the problem of this dissertation.

The research results presented in this chapter have been included in a *Clarivate Analytics Web of Science* databases referred publication (Vasjanov & Barzdenas 2018, Oct.) with a citation index.

1.1. Radio Frequency Power Amplifier Architecture Review and Possible Vectors for Improvement

The first most primitive radio transmitter that was used for telegraphy has been developed in the early 1890s by Guilielmo Marconi. This invention spawned the wireless telegraphy or "spark" era, named due to the transmitter having spark gaps and lasted for several decades. As a result, this became the starting point for the search of more efficient and rapid ways to exchange wireless information (Hansen, 2016). Since then, different ways of transmitting information have been proposed, including the introduction of amplitude modulation (AM) and phase modulation (PM). However, the largest leap in the domain of wireless information transfer has started with the invention of the transistor, as this allowed research and development of portable devices. This lead to the launch of the first commercially automated cellular network (the 1G generation) in Japan in 1979 (Afolabi et al., 2018) and evolved into the currently widespread 3G and the maturing 4G technology. This is possible due to the massive growth in the global mobile communication sector revenue, which increased from €174 billion in 2010 (Wang et al., 2014) to €2.7 trillion in 2017 and is expected to reach over €4 trillion by 2020 (Mobile Industry Observatory, 2017). Moreover, the 1G to 4G leap from a technological standpoint is very substantial, as it transformed the wireless mobile network form a pure telephony system with only voice and primitive text to a universal network that can cope with transporting rich multimedia content in a high-density network. The most recent 4G wireless systems employ and advanced radio interface with orthogonal frequency-division multiplexing (OFDM), multiple-input multiple-output (MIMO) and link adaptation technologies and can support data rates up to 1 Gb/s of low mobility (local wireless access) and up to 100 Mb/s for high mobility (mobile access). However, even with the latter throughput, the increasing number of mobile network users push the envelope even further. The most crucial challenges in the strive to increase the capabilities of future mobile networks are physical scarcity of RF spectra allocated for communication, energy consumption reduction and extending hardware capabilities to guarantee smooth user experience in high-speed applications independently of protocol or frequency band (Wang et al., 2014; Parssinen, 2011). This requires not only innovative solutions employing new modulation schemes and protocols, but also drastic changes in design of the cellular architecture as a whole and each device in particular.

It is widely known that the RF PA is the most power-hungry component in radio transceivers, and is one of the most critical building blocks in radio front-end. Hence, research in this area will help drive overall 5G network costs down while achieving improved energy efficiency (Cheng et al., 2015). Moreover, as technology advances, digital circuits can replace more and more analog circuits

in the RF transceivers. Intermediate frequency (IF) transceiver circuit blocks, such as filters, is a vivid example. Modern RF transceivers can have both analog and digital IF filters, but analog circuit design and, most importantly, layout cannot be automated, whereas the one can synthesize a digital signal processor (DSP) and implement the required filtering capabilities later. Thus utilizing either analog IF filters, or implementing filters in the digital domain, or even having the benefit of both is dependent on the designer's choice and the stringency of the restrictions (transceiver specifications, physical chip layout space, design costs and time, etc.). The RF PA, on the other hand, alongside with the low noise amplifier (LNA) is an RF high-end circuit block which directly links the transceiver and the antenna and their role is irreplaceable. In other words, the RF PA cannot be digitized and will be a constant component in any current and future transceiver.

A research study has been conducted in (Cheng et al., 2015), which focused on investigating the development trend of RF PAs – more than 1000 papers relevant to RF PA study have been statistically analyzed to reveal research trends (Fig. 1.1).

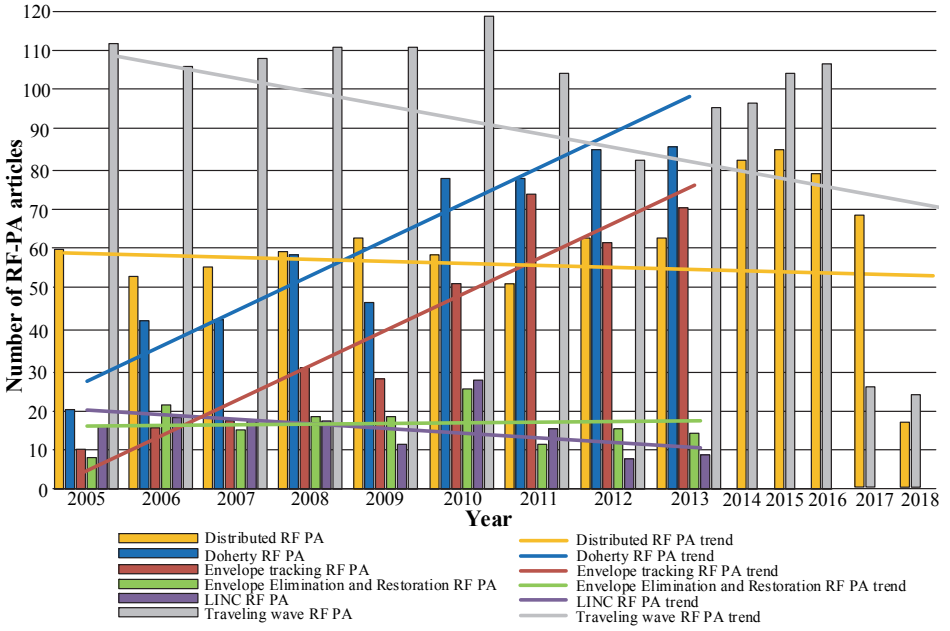


Fig. 1.1. Radio frequency power amplifier research trends

The scope of the latter research, which is based mainly on articles published in different IEEE journals, spans from papers published in 1969 to the ones published in 2014. The results depict not only the overall number of papers relevant to exploring new approaches to RF PA design over the years, but also

describes the globalization, cooperation across affiliations, research cycle and architecture trends. RF PA research trends published in (Cheng et al., 2015) have been updated with two more architectures that have not been included. The updated trend histogram is presented in Fig. 1.1.

Various advanced PA architectures have been proposed throughout the years and demonstrated for increasing RF PA efficiency without losing linearity or even with improved linearity, including envelope elimination and restoration (EER), envelope tracking (ET), LINC, Doherty (DPA) and two additional architectures have been added to the original RF PA research trend histogram published in (Cheng et al., 2015) – traveling wave (TW PA or TWA) and distributed power amplifiers. More than 1400 articles in IEEE journals have been analyzed in order to find out the trend of researching TWA and distributed PA from published from 2005 to 2018. Essentially, TWA and distributed PA (from this point forward, the latter RF PA architecture will be referred as TWA) are identical and use the same approach of incorporating transmission line theory into traditional PA design in order to maintain constant gain and high input (S_{11}) and output (S_{22}) impedance matching values. Therefore, if added up, the common TWA architecture research trend line is constant and higher than those of other PA architectures. The second highest RF PA architecture is DPA architecture, which is getting increasing amount of attention in the past years. The rate of interest for ET PAs is identical to that of the DPA, although the number of articles published each year is significantly lower. LINC and EER architecture PAs are least mentioned in papers due to their practical implementation restrictions. A tendency of mixing advanced architectures in a single solution, for example the DPA features with the advantages of the TWA, has also been spotted although these articles are not included in Fig. 1.1.

The results depicted in Fig. 1.1 clearly define advanced RF PA architectures which are the most promising to be implemented in the next generation wireless systems and they will be discussed in detail in the next chapters.

1.1.1. Radio Frequency Power Amplifier in a Modern Wireless System

Multi-standard connectivity has become de-facto for smart phones and laptops but is emerging also to other more specialized gadgets like e-book readers. Such devices need to be designed for the best performance even when multiple wireless standards are operating simultaneously (Parssinen, 2011).

Concepts, like Internet of Things (IoT), Machine to Machine (M2M) communication, Software Defined Radios (SDR), MIMO systems and cloud-based services are rapidly emerging being integrated in the most common household items.

Therefore, on the one hand there is a need of high complexity hardware and software for multistandard multifunctional devices (such as smartphones, computers, mobile base stations, etc.), but on the other – cheap and power effective solutions are required to provide simple everyday items with wireless connectivity. Moreover, as the modern wireless multistandard environment grows in size, the whole system architecture and the architecture of every single transceiver become crucial and, if addressed incorrectly, might become a bottleneck in the future. Cell planning (CP) is the most important phase in the life cycle of a cellular system as it determines the operational expenditure (OPEX), capital expenditure (CAPEX), as well as the long-term performance of the system. Therefore, it is not surprising that CP problems have been studied extensively for the past three decades for all four generations of cellular systems (Taufique et al., 2017).

Modern wireless systems are migrating from discrete component transmitter and receiver chains to monolithic transceivers. Although the latter integrated circuits (IC) are usually cheaper and smaller in size than their discrete counterparts, the overall architecture tends to stay the same with minor differences.

The main function of a receiver is the demodulation of a wanted signal in the presence of undesired interferers and noise. Due to strong attenuation during air transmission, the RF signal has to be amplified and recovered. Taking into account scenarios with varying attenuation, a wide dynamic range is required for the detection of signals with high data rates. Power consumption is an important issue for receivers. Even if there is no active communication, receivers can't be switched off completely as they have to detect when a transmitter requests a data transmission and subsequently must switch on the receiver chain by means of a wake-up circuit. Consequently, if not active, a receiver has to operate in a standby mode, where the direct current (DC) power is reduced. Nevertheless, accumulation of the drawn DC power over a long stand-by-time can result in significant power consumption. Thus, mobile receivers must have a low power consumption in the stand-by mode (Ellinger, 2010).

The three primary functions of common transmitters are modulation, frequency conversion and power amplification. Consequently, the key performance parameters are modulation accuracy, spectral purity and RF output power. Since a strong signal is locally available, band selection and noise are not as critical as in receivers. Moreover, the variation of the signal level is small thus relaxing the requirements in terms of the dynamic range. As a result, transmitters are less complex and are found in a smaller variety of approaches compared to receivers. High output power signal generation leads to a high DC power consumption, thus, in active operation, the power consumption of transceivers is determined by the transmitter rather than by the receiver. Various modulation

modes with both constant and variable signal amplitude can be employed to transmit data. The first scheme is more power efficient, whereas the latter one is more spectral efficient at the expense of challenging requirements in terms of linearity (Ellinger, 2010). Because of its high performance, the superheterodyne is presently the dominant architecture for both transmitters and receivers and as a result – in modern transceivers (Lee, 2003). A simplified block diagram of the modern transceiver is presented in Fig. 1.2.

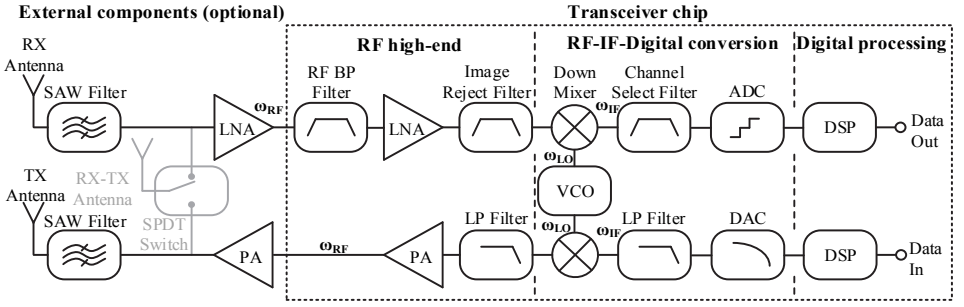


Fig. 1.2. Modern transceiver block diagram

The modern transceiver contains almost all components critical to wireless communication inside a single IC. The latter IC holds circuit blocks that can be divided into three categories – RF high-end blocks, RF to IF to digital conversion circuits and the digital processor. Low noise and power amplifiers alongside with filters make up the RF high-end circuit. RF conversion to digital domain is comprised of a down/up-converting mixer, IF filters and an analog-to-digital (ADC) or digital-to-analog converter (DAC), depending on whether it is a receiver or transmitter chain. The DSP can be either a microcontroller unit (MCU), a field programmable gate array (FPGA) or a DSP depending on the level of computational power required and chip space available.

Modern wireless networks comprise of different output power and number of user supporting radio access nodes called cells (Johansson & Fritzin, 2014). Due to recently increased capacity, a shift in cellular network infrastructure deployment is occurring away from traditional (expensive) high-power tower-mounted base stations and towards heterogeneous elements. Examples of heterogeneous elements include micro-cells, pico-cells, femto-cells, and distributed antenna systems (remote radio heads), which are distinguished by their transmit powers/coverage areas, physical size, backhaul, and propagation characteristics. This shift presents many opportunities for capacity improvement, and many new challenges to co-existence and network management (Ghosh et al., 2012). To accommodate high mobility users in a heterogeneous network, such as

users in vehicles and high-speed trains, a paper (Wang et al., 2014) proposed the mobile femtocell (MFemto-cell) concept. All latter cell types essentially define the radiated RF power, which directly affects the PA requirements. For example, the maximum acceptable path loss required to deliver an adequate pilot channel signal quality $\left.\frac{E_e}{N_0}\right|_{femto}$ is then given by:

$$L_{\max} = 10 \cdot \log_{10} \left[\frac{P_{\max}}{N_{\mathrm{UE}}} \cdot \left(\frac{p_{\mathrm{CPICH}}}{\left.\frac{E_e}{N_0}\right|_{\mathrm{femto}}} - 1 \right) \right] (\mathrm{dB}), \tag{1.1}$$

where $P_{\max}$ is maximum power transmitted by the femto-cell, N_{UE} is the user equipment receiver noise power and p_{CPICH} is the proportion of the femto-cell power allocated to the pilot channel. As a result, coverage levels well in excess of that required for a local connection are achieved at transmit powers below −10 dBm (0.1 mW). For comparison, a *Wi-Fi* access point typically transmits at +20 dBm (100 mW) and phones typically transmit at up to +24 dBm (250 mW) (Saunders et al., 2009). Therefore, femto-cell transceiver PA output power specification can be relaxed and scalable complementary metal-oxide semiconductor (CMOS) processes become very attractive.

Analyzing macro-cells, such as mobile base stations, the power requirements are very different and can go up to tens and even hundreds of watts. This requires devices that have a high breakdown voltage and with enough gain at high frequencies. As a result, medium and high power PAs are usually implemented in *III-V* semiconductors (Lie et al., 2016). The highest powers from hundreds of watts up to kilowatts at frequencies above 1 GHz are obtainable using *GaN*, *Si* bipolar junction transistor (BJT) and *GaAs* process devices (Souza et al., 2014; Komiak 2015; FitzPatrick, 2017). The downside to the latter processes is that it is not possible to include performance-enhancing functionality, including complex bias circuitry, self-testing or calibration capabilities as well as high-density digital processors. This can be further seen, that there are only a handful of papers (up to the year of 2019) on *GaAs*/*GaN* and other *III-V* semiconductor based transceivers published. Moreover, the articles published under the latter conditions present only an integrated high-end part (mixers, amplifiers and biasing) without any digital capabilities (de Sousa et al., 2004; Villain et al., 2000; Boveda & Ortigoso, 1995; Liberati & Calori, 2008; Lim, Lee et al., 2017; Dyadyuk, Shen & Stokes, 2014). An article (Pettenpaul, 1998) provided a discussion on the application of hetero-devices in *GaAs* and *Si* and can be summarized as follows:

1. *SiGe* will result in only minor improvements conceming the known cellular and cordless phone systems, i.e. will not substitute any *Si* Bipolar circuit due to higher cost.
2. *GaAs* HEMT technology is the best microwave material up to 100 GHz. It combines the advantages of unipolar transistors with outstanding performance down to 1.5 V supply but with a twice as higher wafer cost compared to *GaAs* MESFET and even more compared to that of CMOS.
3. The *GaAs* HBT process is a candidate for mobile communication PA's with good *PAE* and the advantage of a single supply voltage. Disadvantages to *GaAs* MESFET and HEMT are reduced shrink potential due to thermal problems, reduced linearity of a bipolar transistor and cost levels comparable to HEMT.

Due to high digital capabilities and self-calibration features being necessary in modern wireless equipment, high power devices are usually discrete and only used in stationary wireless nodes, such as macro-cells. The high-power cell transceiver generates an RF signal but requires one or several stages of external power amplification before the signal is fed into an antenna, as shown in Fig. 1.2 (Zampardi, 2010). Other external components, such as surface acoustic wave (SAW) filters, switches, LNAs and the antenna configuration is totally dependent on system requirements and can differ from the one shown in Fig. 1.2.

Even though the price of implementing ICs using *III-V* semiconductors is substantially higher than that of CMOS process, the latter can't meet the power added efficiency (*PAE*) at a given output power 1 dB compression point (*P1dB*) criterion especially at frequencies above 1 GHz (Niknejad, Chowdhury & Chen, 2012). Therefore, CMOS process is not very suitable for the medium-high power range. On the other hand, pushing mobile devices to lower powers is useful from a design perspective as non-PA components (such as controllers, transceiver blocks, switches, etc.) can readily be integrated with the PA in a single chip (Zampardi, 2010). Therefore, a low power cell, such as a femto-cell, utilizes a single agile transceiver IC alongside a few external components, such as single-pole dual-throw (SPDT) switch with an antenna, ignoring the external PA, LNA and their corresponding antennas (Fig. 1.2 in grey).

Power devices for wireless applications have come a long way since the early '90s, driven primarily by the explosion of high-speed communication systems permeating almost every aspect of day-to-day life. Wireless systems require different RF PAs whose design involves conflicting the main requirements, such as efficiency, linearity and gain (Souza et al., 2014). Among other RF PA requirements, there are parameters like gain control, impedance matching bandwidth. Different compensation schemes, such as unifying the phase shift for

different frequency signals in a broadband PA or linearization, are also worth considering.

The main parameters of the PA, their improvement techniques and circuits as well as various advanced architectures with potential to be implemented in next generation wireless networks are discussed in the following chapters. It is to be noted, that the research focus of this dissertation and main scope of reviewed papers are PAs implemented in scalable processes CMOS and *SiGe* BiCMOS with output powers suitable for portable wireless devices under 32 dBm (1.5 W).

1.1.2. The 5G Wireless Realm

5G is the next leap in the evolution of wireless communication, which introduces many improvements to the existing telecommunications industry, but also comes with various challenges. This emerging technology provides low latency, ultra-high-speed massive connectivity between devices leading to cross-industry transformations, pervasive processing in an ecosystem, where all devices are interconnected (Sarfaraz & Hammainen, 2017). Organizations like The European Conference of Postal and Telecommunications Administrations (CEPT) (The European Conference of Postal and Telecommunications Administrations CEPT, 2018) and Federal Communications Commission (FCC) (Federal Communications Commission FCC, 2018) allocate 5G frequency bands in Europe and USA accordingly. The 5G band licensing per geographical area is presented in Figure 1.3 (everythingRF, 2018).

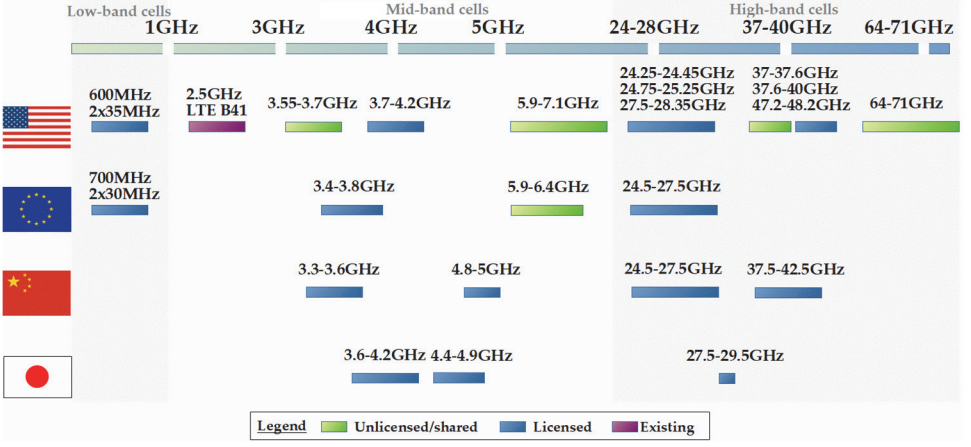


Fig. 1.3. 5G band licensing per geographical area

3GPP standard (European Standards Organization ETSI, 2018) divides the licensed bands into two groups, named FR1 (sub-6 GHz) and FR2 (above

24 GHz). The latter standard doesn't include unlicensed bands both in Europe (5.9–6.4 GHz) and the USA (5.9–7.1 GHz). The unlicensed bands are included in the FR1 range as they serve the main purpose of broadband radio service and are named mid-band 5G frequency range (Qualcomm Technologies Inc., 2017). Therefore, licensed and unlicensed frequency band allocations in the USA, Europe and Asia (only China and Japan are included) can be divided into three regions: low frequency (600–700 MHz), mid-band (1–7.1 GHz) cells as well as high-band cells (above 24 GHz). Low frequency bands (below 1 GHz) are intended to be used for traditional local coverage applications, Internet of Things (IoT), vehicle-to-everything (V2X) and transport infrastructure. The mid-band (up to 7 GHz) can be used for higher throughput data transfer, whereas the high-band will allow for wireless hotspots to emerge and mm-wave sensors to be included in V2X concept (GSMA Spectrum, 2016).

Other 5G specifications include user experienced data rates in the region of 100 Mbit/s to 1 Gbit/s; connection density of 1 million connections per km^2; intermediate frequency bandwidths of up to 150 MHz; portable device maximum output power of 24 dBm (251 mW) end-to-end latency in the millisecond level; and mobility up to 500 km/h (The European Conference of Postal and Telecommunications Administrations CEPT, 2018, Qualcomm Technologies Inc., 2017).

1.1.3. Radio Frequency Power Amplifier Fundamental Metrics

The RF PA, as any other circuit block in electronics, is characterized by a specific set of parameters, which not only reveal its performance and conditions of operation, but are also used for comparison to others of the same application. The main RF PA parameters are distinguished and discussed in this chapter.

Power amplifier class. The commonly used RF PA biasing configurations lead to different amplifier classes, such as *A*, *B*, *AB*, *C*, *D*, *E*, *F*, and *S* class. Linear amplification is represented by *A*, *B*, or *AB* class amplifiers and the active device acts as a current sink/source. Nonlinear signal amplification is performed in class *C*, *D*, *E*, *F*, and *S* amplifiers, which are known as switch-mode amplifiers and the active device is used as a switch (Eroglu, 2016). Highly linear PAs are also the least efficient and vice versa. The main difference in RF PA classes is the tradeoff in efficiency or linearity therefore, the latter two parameters can define the application of an amplifier. For example, a highly efficient class *C* PA can't be considered if amplitude modulation scheme is applied to the signal carrier (Walker, 2012). A summary of RF PA classes versus active device conduction angle and input signal overdrive is presented in Fig. 1.4.

Efficiency Metrics. The RF PA is implemented as a subsystem and consumes most of the DC power from the supply. As a result, minimal DC power

consumption for the amplifier becomes important directly affects the overall RF PA efficiency.

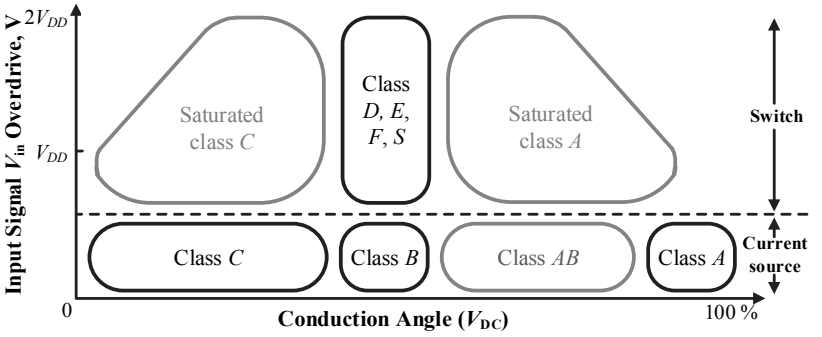


Fig. 1.4. Power amplifier class summary

Amplifier efficiency can be defined by the drain efficiency η_{drain} for metal-oxide field effect transistor (MOSFET) or collector efficiency $\eta_{\text{collector}}$ for a bipolar junction transistor (BJT) and is expressed as

$$\eta(\%) = \frac{P_{\text{out}}}{P_{\text{DC}}} \cdot 100 \,. \tag{1.2}$$

Efficiency in terms of gain can be put in the following form

$$\eta(\%) = \frac{1}{1 + \frac{P_{\text{out}}}{P_{\text{DC}}} - \frac{1}{G}} \cdot 100 \,. \tag{1.3}$$

Eq. (1.2) and Eq. (1.3) do not include the signal power that drives the PA. When RF input power is included in the calculation, the efficiency is then referred to as power-added efficiency η_{PAE} and is expressed as

$$\eta_{\text{PAE}}(\%) = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \cdot 100 = \eta \cdot \left(1 - \frac{1}{G}\right) \cdot 100 \,. \tag{1.4}$$

Transmit Power Levels and Power Output Capability. RF PA output power is a parameter that is highly dependent on the target wireless standards and documents regulating licensed and unlicensed RF device specifications. Moreover, the same wireless standard can have different bands with different maximum power levels and described with their own spectrum emission mask. Fig. 1.5 presents the wireless standard allocation on the RF spectrum and the corresponding maximum transmit power for mobiles devices. The latter figure depicts both licensed (ex. LTE) and unlicensed (ISM) band power specifications. The typical output power is usually around 24 dBm (250 mW) under the according modulation scheme, but can go up to 30 dBm (1.5 W) or even 39 dBm

(8 W) (Ruiz & Perez, 2014); European Standards Organization ETSI, 2016, 2018; Mazar; Electronic Communications Committee ECC, 2016; LG Niviuk, 2019).

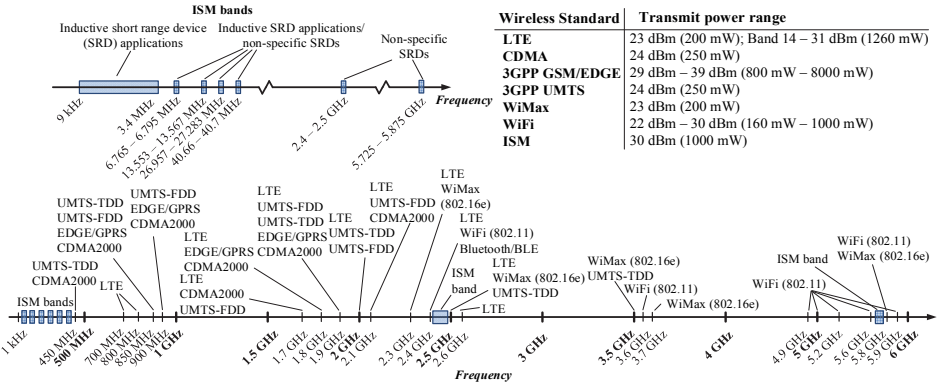


Fig. 1.5. Radio frequency spectrum allocation and maximum transmit powers

The power output capability of an amplifier is defined as the ratio of the amplifier output power to the maximum values of the voltage and current that the device experiences during the operation and is described by the following equation:

$$c_{\mathrm{p}} = \frac{P_{\mathrm{out}}}{N \cdot I_{\max} \cdot V_{\max}}, \tag{1.5}$$

where N is the number of transistors that make up the PA, P_{out} is the output power, $I_{\max}$ and $V_{\max}$ are maximum PA currant and voltage accordingly.

It should also be noted, that wireless standards use different modulation schemes and the signal power under those conditions is not the same as the power of a sinusoidal (otherwise referred as continuous wave signal, CW) signal. The output power of a CW signal is given by

$$P_{\mathrm{out}} = \frac{V_{\mathrm{out}}^2}{2 \cdot R_{\mathrm{load}}}, \tag{1.6}$$

where V_{out} is the output RF signal and R_{L} is the load impedance (usually 50 Ω).

When the signal is modulated, the power becomes a function of time and even though Eq. (1.6) is true for any given time point, it doesn't depict the average power. Given the statistical distribution of the instantaneous output power, which is dependent on the modulation scheme, the average output power can be calculated as

$$P_{\mathrm{out\ avg}} = \int_0^{\infty} \phi(P) \cdot P dP, \tag{1.7}$$

where $\varphi(P)$ is the probability that the output power is between P and $P+dP$ (Shirvani & Wooley, 2003). In practical PA measurements, the given average

output power is measured with the infinity limit replaced by a lengthy signal, which results in $P_{\text{out avg}}$ that includes the nonlinearities of the given amplifier. The latter would be another function of output power under the integral, but is not included in Eq. (1.7).

Stability. Large signal levels, transistor core and package parasitics, magnetic coupling or PA nonlinearities may push the PA into an unstable region and make it oscillate. A practical and common parameter used to determine the stability of an amplifier is the Rollett stability factor or stability factor *K*. Stability factor *K* ensures unconditional stability criteria based on the *S*-parameters of an amplifier modeled as a 2-port network, no matter what passive matching is placed at its input or output (Ruiz & Perez, 2014). Eq. (1.8) and Eq. (1.9) describe the conditions that must be fulfilled.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12} \cdot S_{21}|} \Rightarrow K > 1 \text{ and} \tag{1.8}$$

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21}. \tag{1.9}$$

The *K* factor has limitations related to the dependency of output power levels and the fact, that *S*-parameters are a function of frequency. Therefore, for unconditional stability, the PA must be tested out under different output power levels in a particular frequency range. Moreover, this stability factor analysis does not ensure unconditional stability for multistage PAs (Cripps, 1999; Jackson, 2006, Narhi & Valtonen, 1997). Therefore, even though multistage PAs can be described as a two-port network, other types of analysis such as transient or harmonic balance (*HB*) must be considered during the design phase to ensure stability.

Gain. RF PA can be described in terms of voltage and power gain is defined as the ratio of the output voltage or power to the input voltage or power accordingly, as given in Eq. (1.10) and Eq. (1.11).

$$A_V(\text{dB}) = 20\log\left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) \text{ and} \tag{1.10}$$

$$A_P(\text{dB}) = 10\log\left(\frac{P_{\text{out}}}{P_{\text{in}}}\right). \tag{1.11}$$

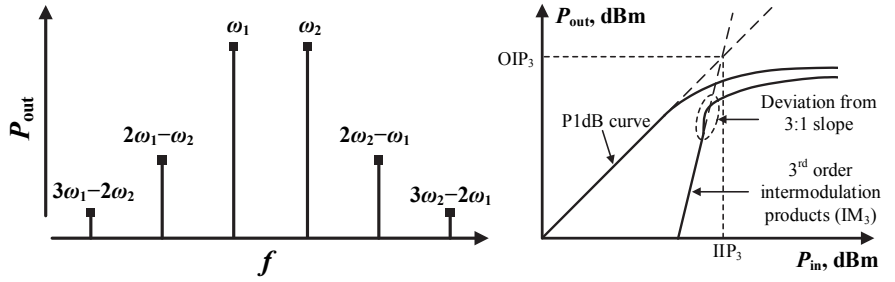
It is possible to obtain higher gain level when multiple amplifiers are cascaded in a multistage amplifier configuration where, if the gains of each stage are given in decibels, the total gain is the sum of individual PA gains (Eroglu, 2016).

AM–AM and AM–PM distortion. AM–AM distortion is referred as the change in output signal amplitude as a function of the input signal level. AM–PM distortion refers to the change in the phase difference between the output and input signals as a function of the input signal level. Saturated power P_{sat}, 1 dB

compression point (*P1dB*) and intermodulation products are the main distortion parameters. The *P1dB* value represents a practical limit between the linear and the nonlinear region of a PA, however, in practice PA output power levels considered acceptable for many communication standards are well below the *P1dB*.

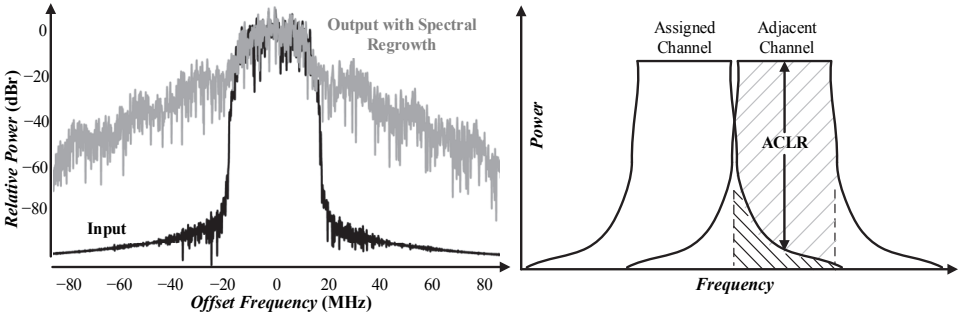
The P_{sat} parameter indicates the maximum output power that a PA can achieve, but working at this power level, the PA is extremely nonlinear with a power gain value that is much lower than the linear gain at low power levels. *P1dB* curve is presented in Fig. 1.6b. If two carriers or tones, usually close in frequency, are applied to the input, the nonlinearities of the PA are reflected in the appearance of several distortion products of different orders. The ones that are of interest due to their possible detrimental effects during RF PA design and research are the intermodulation products (*IMn*), which are odd order products close to the fundamental carrier. The third order products (*IM3*) are placed at frequencies $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$. Higher order products such as the fifth order intermodulation products (*IM5*) at frequencies have smaller amplitudes and are more distant from the fundamental carrier (Fig. 1.6a) (Ruiz & Perez, 2014). At higher output power levels the actual *IM3* curve of the amplifier deviates noticeably from the 3:1 slope as a consequence of high order products affecting the theoretical 3:1 line (Fig. 1.6b). This deviation from the theoretical slope in the high power levels of the PA makes the *IP3* point a less widespread parameter for evaluating the linearity performance of a PA, however, this type of distortion is of the same nature as spectral regrowth, which is of importance in communication standards.

Other important specifications are the error vector magnitude (*EVM*), which limits the distortion of the transmitter in the modulated channel and power back-off. It must be noted that specifications to wireless standard refer to the transmitter and therefore the values should be shared with all the components of the transmission chain.



(a) (b)

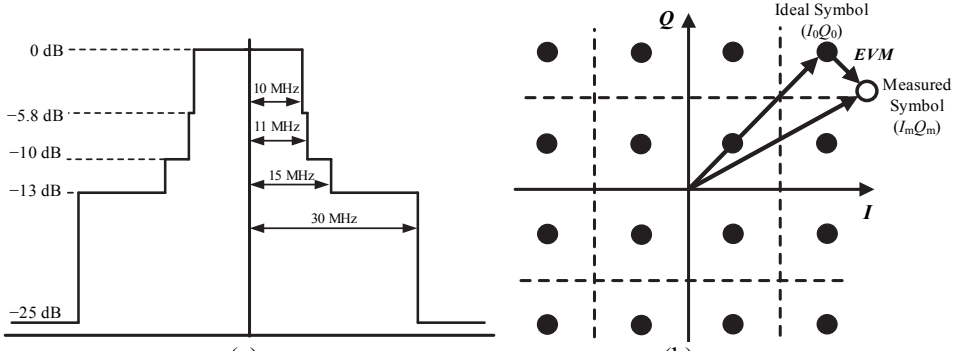
Fig. 1.6. Intermodulation distortion: (a) Two-tone test intermodulation products; (b) 1st and 3rd order intermodulation curves



(a) (b)

Fig. 1.7. RF emission specifications: (a) Spectral regrowth in a 40 MHz channel; (b) adjacent channel leakage ratio in wireless communication

Spectral regrowth is a process when intermodulation band that is generated due to PA nonlinearities stretches n times of the main channel width. In the case of third order distortion products $n = 3$, in the case of fifth order – $n = 5$. Spectral regrowth is unwanted and is regulated by communication standards. Fig. 1.7a presents of the spectral regrowth caused by the nonlinearities of a PA in a 40 MHz 802.11n channel. The spectral regrowth of most concern in a channelized communication standard is the one caused by the third order intermodulation distortion because it lies closest to the main signal. Standards usually limit this spectral regrowth by specifying the *ACLR*. The *ACLR* refers to the amount of power a device transmitting in a channel leaks into its adjacent channel, as seen in Fig. 1.7b.



(a) (b)

Fig. 1.8. (a) Spectrum emission mask of a 20 MHz LTE channel; (b) error vector magnitude concept in a 16QAM constellation

In addition to the above *ACLR* specification, communication standards also set a mask of power levels relative to the power at the center of the channel, and

these limits cannot be exceeded. Fig. 1.8a shows the spectrum emission mask of a 20 MHz channel for the 3GPP LTE standard. As the nonlinearities of PAs cause spectral regrowth, the spectrum emission mask is another specification that must be taken into account when fixing the required linearity of a PA or the maximum available output power for a given PA.

Another linearity metric that can be usually found as a specification in communication standards is the *EVM*. The error vector quantifies the transmit modulation accuracy, as shown in Fig. 1.8b, and it is defined as the difference between the ideal constellation point and the actual transmitted constellation point. The distortion and nonlinearities of the transmitter causes the actual constellation points to deviate from the ideal locations. Specifically, the nonlinearities of the PA cause the *EVM* to degrade so that either the output power must be reduced or the PA linearity improved in order to fulfill this specification. Its value is provided by the standards in decibels or as a percentage, and the standard tends to impose more stringent values as the number of constellation points in the modulation scheme increases (Ruiz & Perez, 2014).

1.1.4. Envelope Tracking Architecture

Dynamic supply or envelope tracking is an efficiency enhancement technique based on the older envelope elimination and restoration (EER) architecture that was proposed by Kahn in 1952. EER architecture has two RF paths – one primary leading to the RF PA input through a limiter and a secondary path on which the envelope of the input RF signal is first detected and further amplified by a highly efficient low-frequency amplifier (LFA), which is also referred to as a modulator (Fig. 1.9a). The RF signal travelling through the main path passes through a limiter that removes the envelope but preserves the phase modulation of the signal. The phase-modulated signal can then be amplified by a highly efficient nonlinear RF PA because the limiter eliminates the possibility of AM–PM distortion in the PA. Finally, the envelope signal and the amplified phase modulated RF signal are combined at the PA by modulating the supply voltage so that amplitude modulation is restored. The main advantage of the EER technique then is the possibility of using highly efficient nonlinear switch-mode RF PAs for variable envelope modulation channels instead of low-efficiency linear RF PAs.
The RF signal in modern fully integrated transmitters doesn't have to be generated and shaped using traditional analog RF chains, containing filters, mixers, voltage controlled oscillators and dividers. Instead, the amplitude and phase information is provided separately in the baseband by a DSP block. This version of the classical EER, shown in Fig. 1.9b, is also known as Polar PA because the baseband signal is converted to a polar format, i.e. amplitude and phase separation, before being amplified.

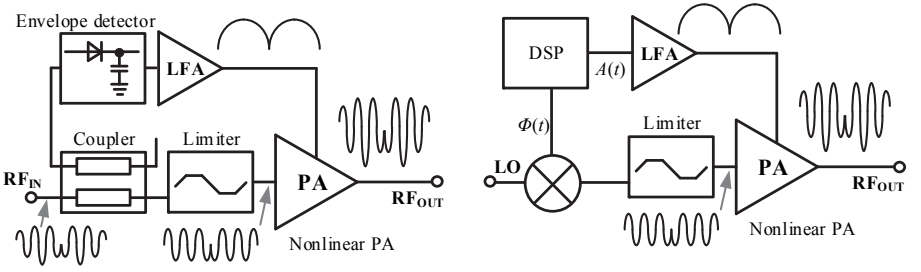


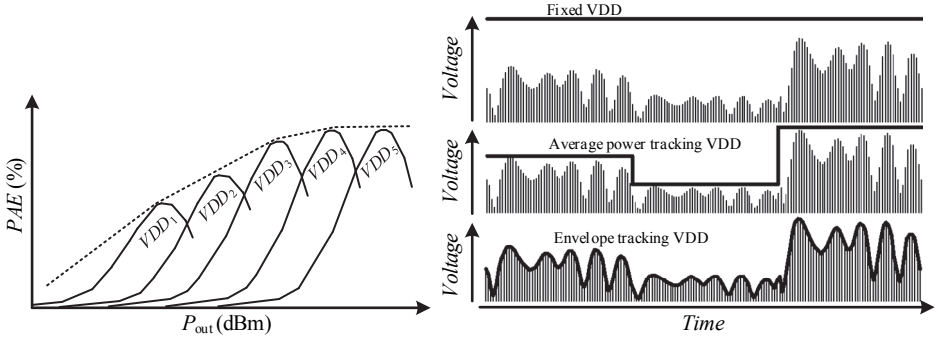
Fig. 1.9. Modulator architectures: (a) envelope elimination and restoration architecture; (b) polar power amplifier architecture

It must be noted that the EER technique has several drawbacks. Firstly, this technique presents dynamic range limitations because the phase modulated RF input signal is amplitude and phase distorted by the RF PA when the supply voltage drops to low values near the transistor V_{KNEE}. Moreover, phase-modulated signals are much wider than required for the original baseband signal and the increased bandwidth requirement poses practical challenges to the ET/EER architecture (Ruiz & Perez, 2014). Therefore PAs exploiting ET/EER architectures are quite narrowband and, as presented in the summary in Table 1.2, the bandwidth doesn't exceed tens of megahertz. Moreover, since only the combination of phase and amplitude restores the original constellation, precise time alignment between the envelope and RF paths is required. For the same reason, the LFA or modulator must generate a suitable supply voltage with great accuracy, requiring both high linearity and great bandwidth. Along with this, the total system efficiency is determined by the product of the envelope amplifier efficiency and the RF PA efficiency, which means that a high-efficiency modulator is critical to the EER technique. High efficiency modulators can be realized in practice with DC-DC converters, but the switching frequency needs to be several times the signal bandwidth as the output ripple must be kept low (Ruiz & Perez, 2014).

The overall efficiency of the ET PA system is roughly the product of the envelope amplifier efficiency and the RF power amplifier drain efficiency, which can be expressed as

$$\eta_{\text{overall}} = \eta_{\text{Envelope ampl}} \cdot \eta_{\text{RF PA}} \tag{1.12}$$

Therefore, the design of the high-efficiency envelope amplifier is critical to the overall efficiency of the ET PA system. The envelope amplifier provides a dynamically changing supply to the RF PA to keep its efficiency higher in the back-off region, as depicted in Fig. 1.10a.

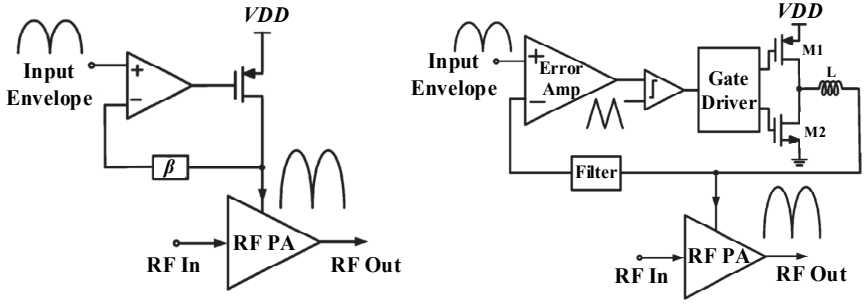


(a) (b)

Fig. 1.10. Power amplifier supply voltage variation techniques: (a) Efficiency as a function of output power for envelope tracking system (Hassan et al., 2012); (b) fixed, average power tracking and envelope tracking supply voltages for a modulated signal

Traditionally, the supply modulator is implemented in the form of a linear regulator (LDO) and since the linear topology has a wide bandwidth and little output ripple, it achieves excellent in and out-of-band spectral performance. The power efficiency of an LDO is poor therefore, it is not well-suited for modern hand held wireless devices processing high *PAPR* signals. A switching ET architecture is an alternative to the linear ET, shown in Fig. 1.11a.

The switching ET, presented in Fig. 1.11b has high efficiency across a broad range of output voltages, but it produces high output ripples and its bandwidth is constrained to be a fraction of the switching frequency, limiting its use to low data-rate systems. A switching regulator can also be used for high data-rate systems but the switching frequency has to be increased. In addition to bandwidth, the modern communication system stringent spectral performance requirements demand even higher switching frequency to adequately suppress the switching ripple.

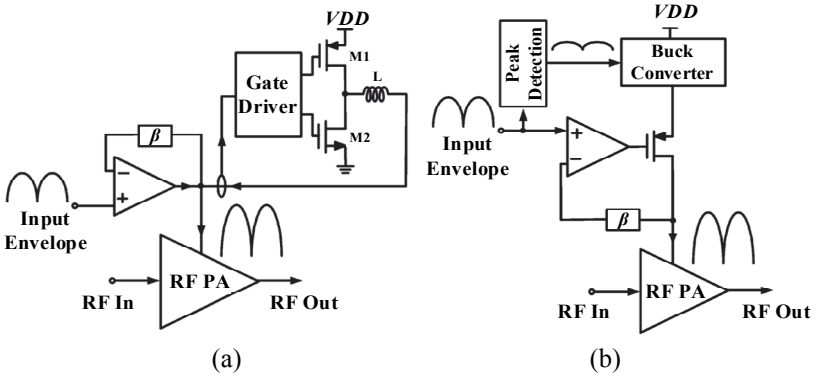


(a) (b)

Fig. 1.11. Conventional envelope amplifier architectures: (a) low dropout regulator amplifier; (b) switching amplifier (Hassan et al., 2012)

However, this causes higher switching losses that severely degrade the overall efficiency (Hassan et al., 2012). The linear and switching ET architectures are two different but still traditional approaches, which paved the way for different architecture derivatives. The latter hybrids are intended to overcome the bandwidth limitation of the switching regulator and poor efficiency of the LDO at back-off. A hybrid regulator can be constructed either by a parallel (Fig. 1.12a) or a series (Fig. 1.12b) connection of the linear and switching regulators, providing a desirable combination of wide bandwidth, low ripple, and high efficiency.

This is reached by means of power distribution – switching regulator provides the average power and a portion of the high-frequency power, whereas the linear one supplies the residual power and acts as an active filter due to its low output impedance. In addition, the linear amplifier absorbs the ripple in the current generated by the switching regulator and achieves an out-of-band noise performance similar to the fully linear ET (Hassan et al., 2012).



(a) (b)

Fig. 1.12. Conventional envelope amplifier architectures:(a) parallel combined linear and switching amplifiers; (b) series combined linear and switching amplifier (Hassan et al., 2012)

Adaptive PA biasing/supply is another technique, which is not a direct member of the ET/EER PA architecture family, but can be mentioned due to the presence of a circuit block that reacts to input signal level and affects the PA operation accordingly. The adaptive biasing architecture is both an efficiency and linearity enhancement technique in which the PA transistor bias is adapted to the amplitude of the input RF signal essentially shifting the operating point across different power classes according to envelope amplitude. In this case, the RF PA is biased at a high quiescent point to provide linear operation only in the high power region.

However, it is not power efficient to maintain the same high bias condition when the transmitted power is low. In this case, a lot of DC power is wasted

through heat as shown in Fig. 1.10b. The same figure presents two approaches aimed at increasing ET PA efficiency. The first is measure the average input power and switch between different power rails. The second approach uses a supply voltage that tracks and imitates the envelope of the input signal. Hence, the low power case, it is possible to ensure the linearity performance of the PA while biasing the PA at lower bias conditions (Ruiz & Perez, 2014).

When adaptive PA supply technique also called multilevel supply modulation (Wang, 2014) is utilized, the RF choke supply voltage varies depending on the input signal power level. Ideally, the supply voltage should vary in small steps, but in this case a high speed DAC is required, which leads to additional efficiency loss. The latter approach is simplified to a comparator switching between several supply rails depending on the input signal power level, which is determined by a power detector. The supply rail changes can induce unnecessary noise into the RF path therefore a smoothing LPF is used in between the LDO and the RF choke. Moreover, the power rail switching algorithm must be time-interleaved with appropriate dead times to achieve the highest efficiency without compromising the reliability of the multimode supply source (Wang, 2014; Vasic, Garcia et al., 2010; Wang, Jin & Ruan, 2016; Sepahvand, Momenroodaki & Zhang, 2016).

A summarized comparison between the reported ET/EER architecture variations is presented in Table 1.1. ET PAs for mobile devices have been demonstrated using *GaAs* HBTs and BiCMOS transistors, showing very high (~50%) overall system (including the PA, modulator and auxiliary circuits) efficiencies. CMOS-based ET PAs are not as efficient as *GaAs* (~30%). Moreover, it is preferred to develop CMOS ET PAs for a maximum supply voltage of 3.4 V and a relatively large knee voltage in alongside with the limitation of FET stacking restrict the overall RF PA performance (Woo, Park, Kim et al., 2014). Since the CMOS PA has a high knee voltage of about 1.1 V, the envelope should be shaped to cover the envelope output voltage spanning from 1.1 V to 3.6 V. The voltage swing range of the modulator (0.4–3.6 V) is larger than the necessary range, and the efficiency is not optimal for the envelope shaping. To optimize the efficiency authors of the paper (Park, Kim et al., 2016) suggest adding a 0.7 V offset voltage to the ground of the supply modulator. This way, the voltage generator with high *PAE* generates the 0.7 V portion of the output voltage and as a result, the overall system efficiency with the proposed modulator is improved by 1.8% point at the peak power compared to that of with the conventional ET supply modulator. At a 10-dB back-off power, the conventional ET supply modulator improves efficiency from 10% to 19% (9% improvement) over the standalone PA, and for the proposed version, the efficiency improves from 10% to 23% (13% improvement). The CMOS PA and ET supply modulator are fabricated in a 0.18 μm RF CMOS technology.

Table 1.1. Envelope tracking architecture feature comparison

Classical linear regulator
• Wideband (tens of megahertz); • Neglectable output voltage ripple (mV range); • Small efficiency at low input signal levels (<<50%); • Regulator efficiency: <60%.
Switching regulator
• Bandwidth is a fraction (several percents) of switching frequency; • Large output voltage ripple (tens of mV range); • Large efficiency at low input signal levels (>70%); • Regulator efficiency: >90%.
Parallel combined linear and switching regulator
• Switching regulator provides average power; • LDO supplies the residual power and acts as an active filter; • Regulator efficiency: 70–90%.
Series combined linear and switching regulator
• Medium output voltage ripple. Larger than that of the linear, but smaller than that of switching (due to the PSRR of the LDO). At high switching regulator frequencies (when the wireless signal has a wide bandwidth) voltage ripples increase (due to the reduction of LDO PSRR); • Regulator efficiency: 60–80% (higher than that of classical linear regulator).
Adaptive PA bias
• No bandwidth restrictions; • No undesired output ripples; • Overall efficiency can be increased at lower input power levels up to 5%.
Adaptive (multimode) PA supply
• Requires high current low loss switches to connect different supply rails to the RF choke and a smoothing LPF to reduce noise; • No bandwidth restrictions; • Output voltage ripple is present during RF choke supply rail change leading to challenges in maintaining fluent switching transition; • Multimode regulator efficiency can reach 97%; • Overall efficiency can be increased by 5–6%.

The ET system has been extensively studied to improve the efficiency as well as apply various functionalities. However, the switching ET PA shows spectral regrowth at the far-out spurious emission domain, and the research for this issue is still insufficient. The far-out spurious noise is reduced by changing the architecture from a linear-assisted switching amplifier to a class *A* mode, but the class-A mode modulator significantly degrades the overall efficiency of the ET PA. The (Kim, Kim, Cho et al., 2012) paper authors propose to add a large capacitor at the output of the ET regulator. The problem with a large capacitive load is that it causes instabilities in the linear regulator, which the authors propose to solve by designing an appropriate *RC* compensation in the linear regulator. The latter paper used an ET architecture presented in Fig. 1.12a. The proposed solution

reduces the *PAE* of the modulator by 2–5%, but the noise performance of the ET PA with the additional capacitor is significantly improved from −108.8/−114.2 dBm/Hz to −130/−133.7 dBm/Hz at 1.93/1.99 GHz respectively.

The hybrid parallel architecture is one of the most popular variation of the ET modulator across multiple (Hassan et al., 2012; Kim, Choi et al., 2010; Jang et al., 2011; Li, Lopez, Schecht et al., 2012; Bondade, Zhang, Ma, 2014) papers as it provides different approaches to efficiency, linearity and noise improvements. A paper (Kim, Kang, Kim et al., 2011) demonstrates that the predistortion technique can be utilized to improve linearity of an advanced PA architecture. The reported ET PA without predistortion has a *PAE* of 37.1% at the peak output power of about 27.6 dBm with gain of about 23.6 dB and an *EVM* of 2.14% (10 MHz LTE signal with *PAPR* of 7.44 dB). The addition of predistortion slightly improved *PAE* to 37.4%, had no effect on the gain and improved the *EVM* by 0.2% at peak output power. Having in mind the fact that the PA doesn't always operate at its peak output conditions, the results seem insignificant. However, ET PA with predistortion has better performance and a lower out-band spectra than the case without, especially at back-off power region.

A summary of papers reporting ET PA research results and parameter improvement solutions, utilizing all architecture variations mentioned in Table 1.1, in CMOS and BiCMOS processes is presented in Table 1.2. The latter summary reveals that ET/EER architecture PAs, as classical DPAs, are narrowband. Even if the PA itself is wideband, the overall bandwidth is limited to the supply modulator, which becomes a bottleneck.

It can be seen, that at frequencies below 1 GHz, the reported signal bandwidth can reach 20 MHz or even 40 MHz. With the increase of frequency, signal bandwidth reduces to 5 MHz. The output power and supply voltages are in the range of portable device specs with the overall system *PAE* of 22–48%. Many papers have been reported where the use of this switched converters in structures such as EER and ET, improve the efficiency of the RF PA in the range 5–20% compared with the classical amplifiers. Nevertheless, in many cases, the use of a linear regulator in parallel with the highly efficient switched converter improves the bandwidth very much by means of a small efficiency penalization (Vasic, Garcia et al., 2012).

The results presented in Table 1.2 can be summarized with the following statements:

1. CMOS process scaling doesn't lead to an increased *PAE*;
2. ET/EER PA designed in CMOS or BiCMOS exhibit largest *PAE* at a supply voltage of 3.3 V;
3. Published ET/EER PAs designed in 0.13–0.32 μm CMOS processes exhibit the best *PAE* at the acceptable process price.

Table 1.2. Summary of reviewed envelope tracking and envelope elimination and restoration power amplifiers in CMOS and BiCMOS processes

Ref.	Process	*VDD*, V	*f*, GHz	P_{linear}, dBm	Overall *PAE*, %	*EVM*, %	Signal *BW*, MHz
(Wu, Lopez & Lie, 2012)	0.35 μm *SiGe* BiCMOS	5	1.85	20.4	22	–	–
(Liu, Wu & Lopez, 2013)	0.35 μm *SiGe* BiCMOS	4.5	0.9	26.5	35.4	3.77	5
(Wu, Li, Lopez & Lie, 2012a)	0.35 μm *SiGe* BiCMOS	4.2	0.75	24	32	5	20
(Lie, Lopez & Tsay, 2014)	0.35 μm *SiGe* BiCMOS	4.2	2.4	24.3	43	5	5
(Li, Ortiz & Spears, 2015)	0.35 μm *SiGe* BiCMOS	3.7	0.7	26.5	42	3.5	10
(Li, Lopez, Lie et al., 2010)	0.35 μm *SiGe* BiCMOS	3.3	1.42	22	33.6	7	5
(Li, Lopez, Wu et al., 2011)	0.32 μm *SiGe* BiCMOS	4.2	2.4	24.3	42	5	5
(Park, Woo et al., 2015)	0.32 μm SOI CMOS	3.9	0.85	26.1	43.8	–	–
(Woo, Park, Kim et al., 2014)	320 nm SOI CMOS	3.4	0.837	25.9	42.3	–	10
(Woo, Park, Kwon et al., 2015)	0.28 μm SOI CMOS	3.4	0.837	25.5	42.2	2.32	40
(Kang, Park, Kim et al., 2013)	0.18 μm CMOS	5	1.85	26	35	–	20
(Kim, Kang, Kim et al., 2011)	0.18 μm CMOS	5	1.85	27.6	37.4	2.34	10
(Park, Kim et al., 2016)	0.18 μm CMOS	4.7	1.7	28.5	36.6	3	10
(Jin et al., 2014)	0.18 μm CMOS	4	1.7	26.5	38.6	3.1	10
(Hassan, Asbeck & Larson, 2013)	0.18 μm CMOS	3.3	2.535	28.3	48	2.1	20
(Hassan, Larson et al., 2012)	0.15 μm CMOS (ET), *GaAs* HBT (PA)	5.5	2.535	23	43	–	20
(Kwak et al., 2012)	0.15 μm CMOS	5	2.5	27.6	46	–	5
(Kim, Choi et al., 2010)	0.13 μm CMOS (ET) *SiGe* HBT (PA)	3.3	1.88	27.8	45	2.98	5
(Francois & Reynaert, 2012)	90 nm CMOS	2	0.93	26	17	5.6	3.84

ET/EER architecture advantages:

1. Various envelope detection methods. Envelope detection can be implemented in the analog domain alongside ET/EER or using a DSP alongside a polar PA architecture;

2. High *PAE* improvement possibilities. Utilizing ET/EER architecture can lead to an overall *PAE* improvement by up to 20% compared to that of the traditional PA;
3. A choice of different architecture variations. Linear, switching and their combinations as well as adaptive biasing techniques are at the disposal of the designer;
4. Linearization possible but difficult as the nonlinearities of other system components such as the regulator have to be accounted for.

ET/EER architecture disadvantages:

1. High synchronization precision between the PA and the regulator requirements. The regulator and the RF path have to be phase matched as the supply voltage must follow the envelope for maximum efficiency;
2. Additional noise in the supply rail due to a switching regulator;
3. Narrow bandwidth. Bandwidth primarily restricted by the regulator therefore is not suitable for multistandard solutions and is not reported to be higher than 40 MHz;
4. Complex implementation. The architecture requires high power regulators with precise controls;
5. No possibility of full integration in a single ASIC. The main reason is the large high current inductor present at the output of the switching regulator.

1.1.5. Outphasing Architecture

Outphasing modulation technique was invented by Henri Chierix in 1935 in order to improve both the efficiency and linearity of AM-broadcast transmitters. Substantially later in the 1970s, its application was extended up to microwave frequencies under the name LINC (linear amplification using nonlinear components). An outphasing transmitter operates as a linear power amplifier system for amplitude-modulated signals having a linear transfer function over a wide range of the input signal levels by combining the outputs of two nonlinear power amplifiers that are driven with signals of constant amplitude but different time-varying phases corresponding to the envelope of the input signal (Grebennikov, 2012).

A simple outphasing power amplifier system is shown in Fig. 1.13a. The signal component separator (SCS) generates from the input amplitude-modulated signal two sine-wave signals of constant envelopes with different phases, $+\varphi(t)$ and $-\varphi(t)$. These two signals are then amplified by nonlinear power amplifiers and added together to produce the output amplitude-modulated signal (Grebennikov, 2012).

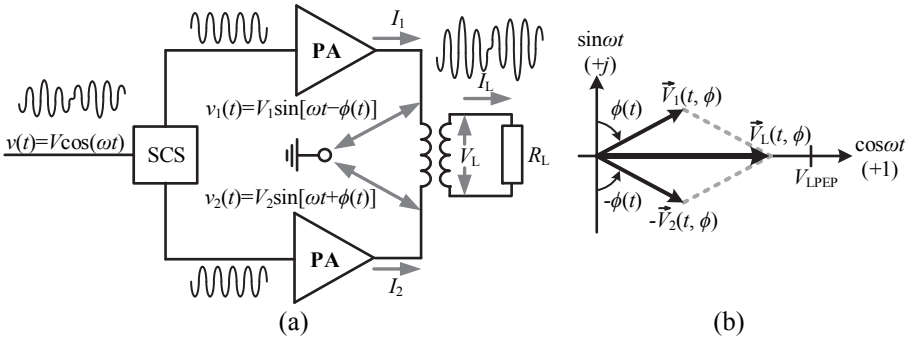


Fig. 1.13. Outphasing power amplifier: (a) concept; (b) output signal formation vector diagram (Bi, 2008)

The AM signal at the input can also include phase modulation and its general mathematical interpretation is as follows

$$v(t) = V(t) \cdot \cos[\omega t + \phi(t)]; 0 \le E(t) \le E_m, \tag{1.13}$$

where $E(t)$ is the real envelope and $\varphi(t)$ represents the original phase modulation in the φ input AM signal. This input signal is separated by the SCS into two constant-envelope PM signals having equal envelopes and opposite modulated phase variations

$$v_1(t) = 0.5 \cdot E_m \cdot \cos[\omega t + \phi(t) + \varphi(t)], \tag{1.14}$$

$$v_2(t) = 0.5 \cdot E_m \cdot \cos[\omega t + \phi(t) - \varphi(t)]. \tag{1.15}$$

Where E_m is the maximum value of time varying envelope amplitude $E(t)$. The outphasing angle $\phi(t)$ is produced by SCS and is expressed as

$$\varphi(t) = \arcsin\left(\frac{E(t)}{E_m}\right); 0 \le \varphi(t) \le \frac{\pi}{2}. \tag{1.16}$$

These two constant-envelope PM signals are separately amplified by two independent identical PAs. The output signals from the PAs are

$$v_1'(t) = A_v \cdot v_1(t) = 0.5 \cdot A_v \cdot E_m \cdot \cos[\omega t + \phi(t) + \varphi(t)], \tag{1.17}$$

$$v_2'(t) = A_v \cdot v_2(t) = 0.5 \cdot A_v \cdot E_m \cdot \cos[\omega t + \phi(t) - \varphi(t)], \tag{1.18}$$

where A_v is the identical amplifier gain. Because of the differential topology of the power combiner, the voltage at the load resistor R_L is

$$v_{\mathrm{out}}(t) = v_1'(t) - v_2'(t) = A_v \cdot \left(v_1(t) - v_2(t)\right) = A_v \cdot V(t) \cdot \cos[\omega t + \phi(t)]. \tag{1.19}$$

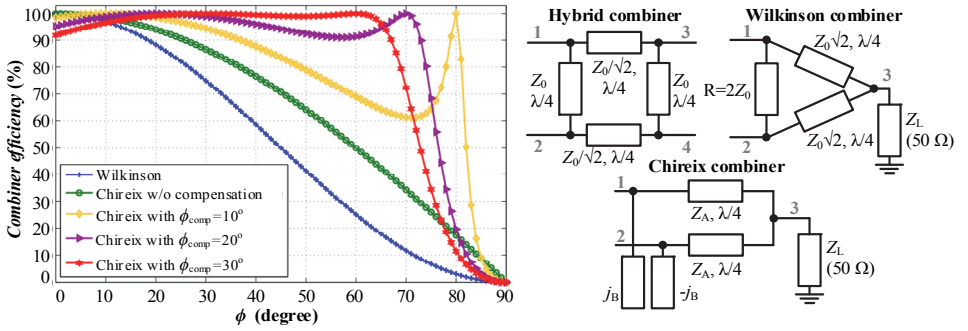
As a result, the final differential signal at the load resistor shows full recovery of the original AM signal (Bi, 2008). The vector diagram of the operation is presented in Fig. 1.13b.

The PAs should be designed to offer the highest possible power efficiency at saturation through the selection of their biasing and impedance matching circuits. This leads to the use of switchmode PAs, that are highly nonlinear but efficient as

well. Careful attention must be paid to the bandwidth response of the PAs, as the LINC separated signals will exhibit larger bandwidth than the original envelope modulated signal; this is due to the added phase modulation. Finally, the power amplification block should be made of two identical or quasi-identical amplifiers to maintain amplitude and phase balance between the two branches.

The use of two highly efficient PAs operated with constant envelope signals in the LINC transmitter does not in itself guarantee that the overall efficiency of the LINC amplifier will be high (Fig. 1.14a). While the amplifiers may operate highly efficiently, it is the remaining available power at the output of the combiner that will determine the overall efficiency of the LINC system (Birafane et al., 2010). Two kinds of combiners are used for this PA architecture: the isolated/lossy combiners (Wilkinson, hybrid) and the non-isolated/lossless combiners (Chireix).

The first class of combining structures is impedance matched, lossy and provides high port isolation. Due to the isolation between the paths, these combiners yield perfect linearity at the output. Their efficiency tends to degrade rapidly, though, as the crest factor of the signal increases. This is due to the out-of-phase components of the combined signals ending up being delivered to the isolated port load in the case of a hybrid coupler and the isolation resistor in the case of a Wilkinson combiner (refer to Fig. 1.14b). This second class of combining structures groups is unmatched lossless outphasing combiners.



(a) (b)

Fig. 1.14. Outphasing power amplifier: (a) combiner efficiencies (Montesinos et al., 2012); (b) Hybrid, Wilkinson and Chireix power dividers (Birafane et al., 2010)

This class includes the lossless Wilkinson-type combiner, that is, without the isolation resistor, and also a combiner that typically includes two quarter-wavelength transmission lines, a tee junction, and shunt reactance of opposite values at the input of each transmission line; this is typically called the Chireix-outphasing combiner (Birafane et al., 2010; Montesinos et al., 2012). Without the shunt opposite value reactances at the input of each transmission line, both

amplifiers experience a complex load $R'_{\mathrm{L}}(\varphi)$ that varies with the out-phasing angle φ, resulting in efficiency degradation. The complex load as a function of the outphasing angle and the compensation shunt reactance, which is usually implemented as a transmission line stub, are described using the following equations:

$$R'_{\mathrm{L}}(\varphi) = \frac{R_{\mathrm{L}}}{2\sin^2\varphi}; \tag{1.20}$$

$$B(\varphi) = \frac{\sin(2\varphi)}{R_{\mathrm{L}}}. \tag{1.21}$$

Furthermore, peak efficiency in other back-off regions can be achieved by using adaptive reactive compensation components (e.g., digital or analog varactors, CMOS/RF-MEMs switches). Nevertheless, the practical Chireix amplifier performance is still limited by the parasitic losses in the reactive matching network and in the power combiner. Causes are the limited quality factor (Q) of inductors and (tunable) capacitors in the reactive matching network as well as ohmic losses (Liu, Schreurs et al., 2010).

A third class of power combiners has been reported in (van Schie et al., 2010) and (Lee, Lee, Paek et al., 2010), which present the transformer-based power combining network. The classical way of realizing this convenience causes the back-off efficiency to be very narrow-band, while power combining in an outphasing transmitter is fundamentally wideband. Moreover, a classical Chireix-outphasing combiner operates only with a single-ended load, whereas the transformer-based is compatible with a differential load. A class *E* outphasing PA reported in (van Schie et al., 2010) shows a 10 dB back-off efficiency is larger than 27.3% over the same bandwidth. The 6 dB back-off efficiency is larger than 46.4% over this bandwidth with the peak output power of 33.9 dBm at 700 MHz. This is one of the highest efficiency values over 10 dB back-off and 29% bandwidth (around 700 MHz) reported.

SCS is realized either in the analog or digital domain. The analog implementation is essentially an AM–PM converter and is complex due to simultanious generation of two signals involving memoryless nonlinear techniques with a high degree of accuracy. Various approaches have been propose, several of which (SCS impemented in analog baseband, analog IF operating in feedback or open-loop topologies) have been mentioned in (Barton & Perreault, 2015), but difficulties remain in terms of factors, such as implementation complexity, bandwidth, and power consumption, owing to the stringent distortion and noise requirements. For a digital SCS implementation, which is currently the most common approach (Barton & Perreault, 2015), arbitrary waveform generators and *I/Q* (In-phase/Quadrature) up-converting

modulators are used to generate the two phase modulated RF input signals (Bi, 2008).

A summary of papers reporting outhpasing PA research results and parameter improvement solutions in CMOS process is presented in Table 1.3. Similar to ET/EER and DPA, the outphasing PA is narrowband. The output power and supply voltages are in the range of portable device specs with the overall system *PAE* varies depending on which class PA is used and is in the range of 16–62%. Moreover, system efficiency greatly depends on the organisation of the DSP algorithm, therefore basic information such as the process, PA class and frequency is not sufficient enough to fully describe *PAE*. The results presented in Table 1.3 can be summarized with the following statements:

1. CMOS process scaling doesn't lead to an increased *PAE*;
2. Comparing to other advanced PA architectures, the *PAE* of an outphasing PA is dependent on the DSP algorithms and wireless standard.

Table 1.3. Summary of reviewed outphasing power amplifiers in CMOS process

Ref.	Process	*VDD*, V	*f*, GHz	*P1dB*, dBm	Overall *PAE*, %	PA class
(Liu, Schreurs et al., 2010)	0.18 µm CMOS	1.8	5.2	17.4	62 (peak)	AB
(Lee, Lee, Paek et al., 2010)	0.18 µm CMOS	–	1.95	26	20	AB
(Lee, Jang & Hong, 2013)	0.13 µm CMOS	3.5	1.95	28.5	29.6	E
(Godoy et al., 2011)	65 nm CMOS	–	2.4	20	27.8	E
(van Schie et al., 2010)	65 nm CMOS	3.6	0.7	33	46	E
(Ghahremani et al., 2017)	65 nm CMOS	1.25	1.4	20	58	E
(Fritzin, Svensson & Alvandpour, 2011)	65 nm CMOS	5.5	1.95	29.7	26.6	D
(Banerjee et al., 2015)	45 nm CMOS	2.4	2.4	31.6	43.7	E
(Hu et al., 2016)	40 nm CMOS	1.2	5.9	22.2	16.1	E
(Xu et al., 2011)	32 nm CMOS	2	2.4	25.3	35	D

Outphasing architecture advantages:

1. Architecture simplicity. Outphasing PA only consists of a SCS, two parallel amplifiers and a power combiner;
2. Efficiency can be increased without hardware changes by means of improving DSP algorithms;
3. Predistortion techniques are applicable in order to enhance overall system linearity;
4. Possible integration in a single ASIC. The main bottleneck is the power combiner.

Outphasing architecture disadvantages:

1. Narrow bandwidth. The main bottleneck is the power combiner;
2. High synchronization precision between parallel RF paths required for maximum efficiency;
3. Practical efficiency, compared to the theoretical, is highly reduced due to losses in passive components;
4. Specific power combiners required. Common power combiners (Wilkinson, hybrid) do not provide sufficient performance, therefore specific phase-compensated are required.

1.1.6. Doherty Architecture

Originally proposed in the early 1936 by W. H. Doherty, widely adopted and thoroughly investigated, DPA was resurrected at the beginning of this century (Colantonio, Giannini & Giofre, 2015). By introducing the Doherty architecture DC to RF conversion efficiencies were increased by a factor of two to over 60% (Pengelly, 2016). In spite of more than 80 years from its introduction, the DPA actually seems to be one of the best candidates to realize PA stage for current and future generations of wireless systems (Cheng et al., 2015). In fact, the increasing complexity of modulation schemes, used to achieve higher and higher data rate transfer in modern wireless systems, is requiring PAs able to manage signals with a large time-varying envelope (Colantonio et al., 2010). The Doherty technique is extensively adopted in *L-S* band applications, typically for base station PA design, demonstrating to be more than a promising solution for modern high performing transmitters. Some interesting results have been demonstrated also for high frequency application, with the realization of monolithic microwave integrated circuit (MMIC) Doherty amplifiers based on *GaAs* devices for *X*-, *Ku*-, and *K*-band or *GaN* devices for backhaul applications at 7 GHz (Colantonio, Giannini & Giofre, 2015).

The Doherty power amplifier is based on the active load concept, to suitable modulate the impedance termination of an active amplifying device, thus forcing the latter to operate at its maximum efficiency condition for a pre-determined range of input and/or output power levels. The standard DPA architecture, reported in Fig. 1.15, is composed by a main (or carrier) amplifier, whose output load is modulated through the auxiliary (or peaking) amplifier (Colantonio, Giannini & Giofre, 2015). The modern DPAs are usually implemented by a proper combination of two active devices designed to operate as a class *AB* (main) and as a class *C* (auxiliary) power stage, respectively. Both PAs are connected at the output through a quarter-wave transmission line ($\lambda/4$ TLine), with the aim to properly exploit the active load modulation concept performed by the auxiliary amplifier on the main one.

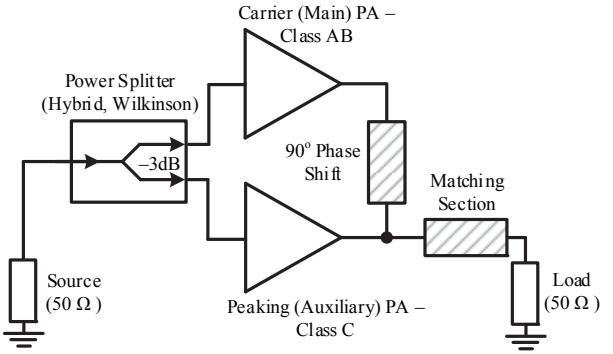


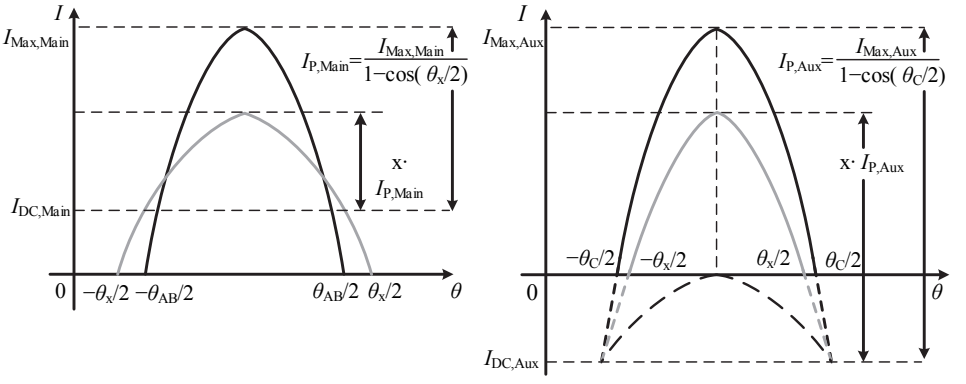
Fig. 1.15. Typical Doherty power amplifier architecture

In any case, the behavioral analysis of the DPA can be performed considering two different operating conditions:

- Low-power, i.e. before the auxiliary device is turned on, which is referred as break point condition;
- Medium-power, when both devices are active, referred as Doherty region.

The device parameters to be considered during the design stage of a DPA are the maximum achievable output current (I_{Max}), the constant knee voltage (V_k) and the pinch-off voltage (V_p) (Colantonio et al., 2010).

The resulting output current waveforms for the main and auxiliary devices are plotted in Fig. 1.16a and Fig. 1.16b respectively.



(a) (b)

Fig. 1.16. Drain current for: (a) the main and (b) the auxiliary devices (Colantonio, Giannini et al., 2008)

For the main amplifier, a generic class *AB* bias condition ξ can be represented by the ratio between the selected bias point ($I_{DC,Main}$) and the maximum drain current value ($I_{Max,\ Main}$) and the resulting current conduction angle (*CCA*) θ_{AB} are given by the following equations:

$$\xi = \frac{I_{DC,Main}}{I_{Max,Main}}, \tag{1.22}$$

$$\theta_{AB} = 2\pi - 2\arccos\left(\frac{\xi}{1-\xi}\right). \tag{1.23}$$

Similarly, for the auxiliary device, a "virtual" bias point I_{DC}, auxiliary can be defined (refer to Fig. 1.16b), which schematizes the actual bias condition required to control its turning on condition with respect to the main. Due to the aux PA starting from different bias levels, different drain currents are reached. The maximum current value for the auxiliary device $I_{Max,\ Aux}$ is usually related to the maximum current of the main device $I_{Max,Main}$ and the output back-off (*OBO*) and is defined as

$$I_{Max,Aux} = I_{Max,Main} \cdot \frac{1-\alpha}{\alpha} \cdot \frac{1-\cos(\theta_C)}{\theta_C - \sin(\theta_C)} \cdot \frac{\theta_{AB} - \sin(\theta_{AB})}{1-\cos(\theta_{AB})}, \tag{1.24}$$

$$OBO = -20\log(\alpha). \tag{1.25}$$

OBO is the parameter, which defines the point when the auxiliary device is turned on and is usually measured in *dB*. A Plot describing the ratio of auxiliary and main device currents versus the main device bias point at different *OBO* is presented in Fig. 1.17a. Moreover, the auxiliary device requires a higher output current when compared with the main one, if the chosen *OBO* value is greater than 5 dB, while its value is smoothly dependent on the main PA bias point. The DPA approach is distinguished from other advanced PA architecture due its load modulation effect (Colantonio, Giannini et al., 2008).

Knowing the current value of the main device I_{Main}, it is possible to compute the values of load resistance $R_{L,Main}$ seen by the main device at the break point and the required characteristic impedance of the output $\lambda/4$ TLine (Z_0) by using the following expressions

$$R_{L,Main} = \left.\frac{\alpha \cdot (V_{DD} - V_k)}{I_{Main}}\right|_{break}, \tag{1.26}$$

$$Z_0 = \frac{(V_{DD} - V_k)}{I_{Main}}. \tag{1.27}$$

Similarly, the resistance seen by the auxiliary device in the Doherty region has to be matched to 50 Ω via an output matching network and is calculated using the following equation

$$R_{\mathrm{L,Aux}} = \frac{V_{\mathrm{DD}} - V_k}{I_{\mathrm{Aux}}}. \tag{1.28}$$

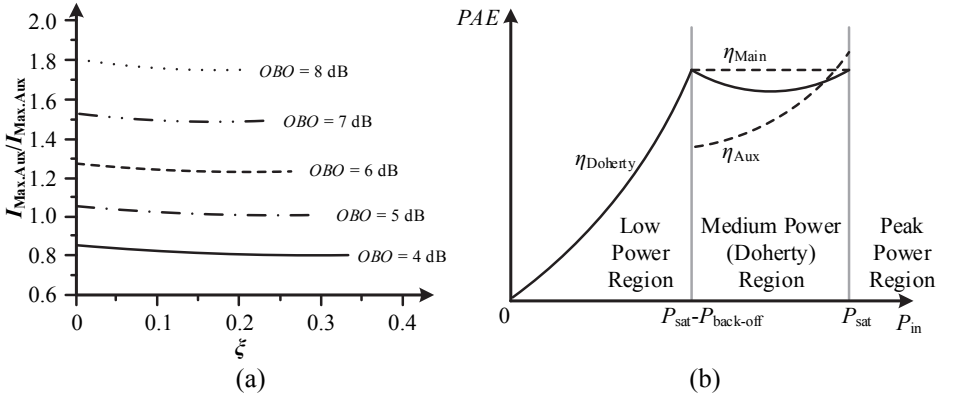


Fig. 1.17. Doherty power amplifier characteristics: (a) ratio between $I_{\mathrm{Max,Aux}}$ and $I_{\mathrm{Max,Main}}$, as a function of the main power amplifier bias point for different *OBO* values; (b) aggregate Doherty power amplifier efficiency (Colantonio, Giannini et al., 2008)

Moreover, the output matching network has to guarantee the compensation of the device output reactance and the short circuit condition for the second and third harmonic components of the drain current waveform, in order to fulfil the "tuned load" condition across the overall nonlinear current source that consists from the main and auxiliary amplifiers (Colantonio et al., 2010).

At saturation, both devices achieve their maximum current. Thus, for the main device the actual value of R_{L} becomes higher due to the current supplied by the auxiliary device, whereas for the auxiliary device the load resistance is reduced. Due to load modulation, the output efficiency is substantially higher than that of a typical class *A*- or *AB*-class PA on a as shown in Fig. 1.17b.

A drawback to the increased efficiency of DPAs is their narrowband nature. The following statement is true due to the limits of the classical $\lambda/4$ output impedance inverter – it can provide proper operation in around 10% bandwidths (Cripps, 2008). Paper (Giofre, Piazzon, et al., 2014) addresses the following issue and proposed impedance inverter topologies that lead to achieve a 560% fractional bandwidth improvement with respect to the conventional approach. This leads to a DPA with 83% fractional bandwidth. The presented impedance inverter concept is based on rearranging the transmission lines that connect both main and auxiliary devices to the load. The presented solution has its drawback,

as the characteristic impedances of the transforming transmission lines are 60 Ω, 121 Ω and 73 Ω (Giofre, Piazzon, et al., 2014). Even though impedance values of 60 Ω and 73 Ω have sufficient current handling capabilities, the 121 Ω microstrip line poses some problems. To achieve such a characteristic impedance at 2.4 GHz, the trace must be around 0.1 mm wide for a 1.6 mm thick PCB with plating thickness of 36 μm and dielectric permittivity of 4.2. A conductor with these parameters can carry around 0.75 A, which is not high, bearing in mind that the auxiliary device can reach currents that are double to the main device current. Therefore non-standard dielectric permittivity materials are required to increase the current handling capability of the conductor. Another paper (Watanabe et al., 2012) proposed an impedance inverter network consisting of lumped components and reached a modest fractional bandwidth of 16%, compared to that reported in (Giofre, Piazzon, et al., 2014).

The output impedance inverter is typically implemented with a quarter-wavelength transmission line, ensuring the reduction of load impedance seen by the main PA when the auxiliary PA turns on. However, a quarter wave TLine is hard to implement in CMOS as the losses would simply be too high (Reynaert, Cao et al., 2016). Several papers (Ryu, Jang et al., 2014; Reynaert, Cao et al., 2016; Kim, Lee & Hong, 2016) report using series combining transformers in order to imitate the loadpull effect. The effect is reduced, comparing to the traditional DPA, but the benefit of combining a Class *AB* and a Class *C* PA still results in a higher overall efficiency and a possibly increased bandwidth. The latter version of DPA is referred to as quasi-DPA (Kim, Lee & Hong, 2016). The same paper reported a quasi-DPA with a 44.4% *PAE* at P_{sat} = 30.7 dBm and a 39.8% at 3.5 dB back-off. The reported quasi-DPA was designed in 0.18 μm CMOS and had a bandwidth spanning from 1710 MHz to 1980 MHz.

Another approach to the form of the impedance inverter, reported in (Watanabe et al., 2012) and (Kang, Yu et al., 2006), is to use lumped components. Paper (Kang, Yu et al., 2006) reports all matching circuits, including quarter-wave transformer and offset part for the time-delay compensation, consisting of lumped components. The PA delivers 22.7 dBm at *P1dB* compression point with 25 dB power gain and 60% *PAE* and the *PAE* at 5 dB backed-off power level shows about 35%.

A summary of papers reporting DPA research results and parameter improvement solutions in CMOS and BiCMOS processes is presented in Table 1.4. It is to be noted, that all DPAs in the latter table are narrowband due to the nature of the architecture and are intended to exhibit maximum performance at a certain frequency. The output power and supply voltages are in the range of portable device specs and the back-off power of 5–10 dB provides overall system *PAE* of 21–51%. The results presented in Table 1.4 can be summarized with the following statements:

1. CMOS process scaling doesn't lead to an increased *PAE*;
2. Supply voltage reduction doesn't necessarily lead to an increased *PAE*;
3. Published DPAs designed in 0.13 μm and 0.18 μm CMOS processes exhibit the best *PAE* at the acceptable process price.

Table 1.4. Summary of reviewed Doherty power amplifiers in CMOS/BiCMOS processes

Ref.	Process	*VDD*, V	*f*, GHz	P_{linear}, dBm	Overall *PAE*, %	Back-off, dB
(Kuo, Lin et al., 2011)	0.35 μm *SiGe* BiCMOS	5	3.5	30	25	10
(Lin, Yeh et al., 2004)	0.35 μm *SiGe* BiCMOS	–	1.95	15	33	8
(Tzschoppe et al., 2014)	0.25 μm *SiGe* BiCMOS	2.5	5.6	22	25	6
(Zhao et al., 2013)	0.25 μm *SiGe* BiCMOS	–	2.4	22.5	21	5
(Choi, Kang et al., 2009)	0.13 μm CMOS (ET), *GaAs* (PA)	3.3	1.8	24.22	38	6
(Kim, Jee et al., 2014)	0.25 μm *GaN*	28	2.14	33.2	51.8	3
(Cui, Roblin et al., 2007)	0.18 μm CMOS	3.7	3.5	24.4	36.1	6
(Ryu, Jung & Jeong, 2012)	0.18 μm CMOS	3.3	2.4	29.5	22	5
(yun Liu et al., 2006)	0.18 μm CMOS	3	2.4	22.6	31	7
(Kim, Son et al., 2014)	0.18 μm CMOS	–	0.89	25	43.6	5
(Ryu, Jang et al., 2014)	0.13 μm CMOS	3.3	2.4	31.9	30.1	5
(Wongkomet et al., 2006)	0.13 μm CMOS	3.3	1.7	31.7	33	5
(Kang, Yu et al., 2006)	0.13 μm CMOS	3	2.4	22	45	7
(Liao et al., 2006)	90nm CMOS	3.3	2.4	30	24	5
(Gaber et al., 2012)	90nm CMOS	2.4	2.4	24.8	26	5
(Carneiro, Deltimple et al., 2015)	65nm CMOS	5.5	2.535	23.4	25	8.5
(Afsahi et al., 2010)	65nm CMOS	3.3	2.4	33.5	20	5
(Deltimple, Carneiro et al., 2015)	65nm CMOS	2.5	2.4	23.4	24.7	7
(Reynaert, Cao et al., 2016)	40nm CMOS	1.5	–	23.4	23.3	6

Main features of the DPA are summarized in the below statements.

DPA architecture advantages:

1. High efficiency – loadpull concept implemented in the DPA utilizes $\lambda/4$ microstrip TLines and lets the designer achieve higher overall *PAE* with

less complex additional circuit solutions (opposed to ET architecture) at any single frequency band. Moreover, DPA is near to its peak efficiency in the whole back-off power range;

2. Linearization techniques, such as feed-forward and predistortion can be easily implemented without any constraints;
3. Simplicity – no complex circuitry reacting to the input signal required (opposed to ET architecture);
4. A combination of multiple PAs in different power classes possible. The traditional DPA consists of the main linear PA and the auxiliary nonlinear one. But DPA architecture is not restricted to only the latter combination, as multiple-way DPAs are also possible where every PA works in a different power class;
5. Lumped and distributed impedance inverters are possible. Both the impedance inverter and the power splitter as well as the delay compensation can be implemented using lumped and distributed approaches.

DPA architecture disadvantages:

1. Increased losses in RF path due to power splitter and combiner;
2. High synchronization precision between RF paths required. Main and auxiliary RF path lengths (delays) must be equal for maximum efficiency;
3. Large overall area. Architecture utilizes a power splitter at the input and a power combiner at the output, both of which have a form factor dependence on the operating frequency;
4. Narrow operating bandwidth due to the nature of the output $\lambda/4$ microstrip impedance inverter. Papers (Giofre, Piazzon, et al., 2014) and (Watanabe et al., 2012) propose methods of increasing the bandwidth, but sacrificing the overall area and stressing the overall manufacturability and current handling capability (non-standard PCB materials with specific dielectric permittivity are required, which increases the price) of the solutions;
5. Low integration potential. Impossible to implement wideband integrated solutions for up to 2 GHz due to large impedance inverter quarter-wavelength values.

1.1.7. Traveling Wave Architecture

Broadband amplifiers are the essential building blocks of high data rate wireless, radar, instrumentation systems and optical communication systems. Deep submicron (0.35–0.11 μm) CMOS technology (E. D. Manolov, 2015) provides the high-speed active devices along with on-chip passives components

required for implementation of the broadband amplifiers. Due to cost and integration considerations, CMOS offers a higher level of integration at a lower cost compared with other high-speed semiconductor technologies such as *GaAs* and *SiGe*. Distributed amplification is considered as a major technique for broadband PAs and with the scaling of CMOS process the achievable unity power gain frequency f_t is tops 100 GHz and allows to design microwave or millimeter wave amplifiers (Moez & Elmasry, 2005; Green et al., 2008; Egels et al., 2005).

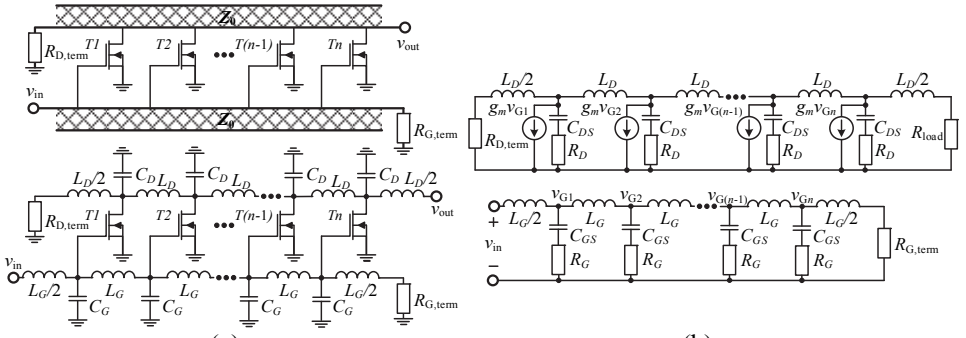


Fig. 1.18. TWA: (a) concept (Moez & Elmasry, 2004) and (b) small signal model (Liu, Lin, Deng et al., 2004)

One particularly effective topology for enhancing communication speed and bandwidth is called distributed amplifier (DA) and is also known as the traveling wave amplifiers (TWA). The conventional TWA topology (Fig. 1.18a) is based on a principle of a ladder LPF that makes up a transmission line with an impedance Z_0 (typically 50 Ω), although (Moez & Elmasry, 2005) paper reported an amplifier based on bandpass filters. Since interconnects with a typical length less than a few hundred microns are not considered transmission lines, the transmission lines are artificially constructed of a ladder of lumped-element inductors and capacitors. Therefore, the analysis and design of CMOS TWA differ from those of conventional discrete microwave TWA. The transmission lines in CMOS technology are artificially constructed of a ladder of inductors and MOS transistor gate-source parasitics acting as capacitors with low equivalent series resistance (*ESR*) as presented in Fig. 1.18b. As a result, this structure does not provide an unlimited bandwidth by acting like a periodical lowpass filter. The maximum bandwidth and the characteristic impedance Z_0 of a TWA is limited to the cutoff frequencies of artificial gate and drain transmission lines and can be expressed as

$$\omega_c = \sqrt{\frac{1}{LC}}; \tag{1.29}$$

$$Z_0 = \sqrt{\frac{L}{C}}, \tag{1.30}$$

where L and C are the values of the inductors and capacitors of the artificial transmission lines. If we assume that the overall size and power dissipation of the amplifier is fixed and is terminated in its characteristic impedance, then the smaller each stage and the higher the number of stages, the larger the ω_c and the larger the DA bandwidth. In reality, the bandwidth is further limited by ubiquitous presence losses throughout the whole structure (including series resistance in the inductors, series resistance in the transistor gates, and transistor output conductance) (Green et al., 2008; Moez & Elmasry, 2004). It is possible to reduce the losses in the transmission line inductors by simply reducing their size, but referring to Eq. (1.30), this reduces the characteristic impedance. In order to compensate this, one can also reduce the capacitance but to a limit of the lowest value of the FET parasitic capacitance (Moez & Elmasry, 2004). A distributed amplifier is called uniform if all transistors are identical. In the case of uniform distributed amplifiers integrating identical transistors, the optimum power load is constant for each drain-line section (Duperrier et al., 2001). It is also worthwhile noting, that the artificial transmission lines are formed both at the TWA input and at the output and depending on the number of identical sections, the overall area can be quite large. Both drain and gate transmission line ends are terminated appropriately to avoid reflections. The voltage and power gain of the conventional TWA is expressed as

$$A_v = \frac{1}{2} n g_m Z_0 \text{ and} \tag{1.31}$$

$$A_P = \frac{1}{4} n^2 g_g^2 Z_0^2, \tag{1.32}$$

where n is the number of distributed stages, g_m denotes the transconductance of each stage and Z_0 is the drain-line termination. In order to increase the gain of the conventional TWA, one should increase the number of stages but due to attenuation on the artificial transmission lines, it is limited to the optimum number of stages, which is given by

$$n_{\text{opt}} \leq \frac{2}{r_g \omega^2 C_{\text{GS}}^2 Z_0}, \tag{1.33}$$

where r_g is the parasitic resistance of the gate and the inductors, ω is the highest frequency of interest, C_{GS} is transistor gate-source parasitic capacitance and Z_0 is the characteristic impedance. Usually the optimal TWA segment number lies in the region of $n_{opt} = [3...5]$ due to a non-proportional gain in bandwidth compared to the losses in efficiency. The theoretical maximum *PAE* of the conventional TWA can be expressed as

$$\eta_{\mathrm{PAE,max}} < \left(1 - \frac{1}{A_v}\right) \cdot \frac{1}{8} n \frac{Z_0}{R_{\mathrm{L}}}. \tag{1.34}$$

Eq. (1.34) indicates that increased periphery per stage helps to increase efficiency if this increased periphery does not adversely affect the gain at highest frequency of interest (Ayasli, Mozzi et al., 1982; Ayasli, Reynolds et al., 1984).

Due to the superior performance in gain, bandwidth, stability, and input-output isolation, the cascode configuration is employed in gain stages in most reported papers that have been reviewed TWAs (Lu, Chen & Lin, 2005; Tarar et al., 2015). However, a conventional distributed amplifier has disadvantages that a half of the input power is wasted in the left termination of drain transmission line and each FET operates under different efficiency conditions. Another issue in design of TWAs is noise of the input termination. For maximum power transfer from antenna to the front-end circuit, a 50 Ω passive resistor is usually employed in to terminate the input transmission line of the low noise TWA (Chen & Wang, 2006; Mesgari et al., 2014). Different variations of non-uniform TWAs, where inductor values or transistor sizing or both are progressively changed and various solutions on terminating both the gate and the drain lines have been proposed.

One of the reported variations of the conventional TWA is called “tapered” TWA, which involves progressively decreasing the inductor value along the output (drain) line. What’s more, the drain transmission line tapering maximizes the forward-traveling wave, while minimizing the unwanted reverse wave. The input signals to all FETs are equalized, since tapering compensates for the line attenuation. For the tapered distributed amplifier, the power gain will be quadrupled, if both the load current and the FET voltage gain are doubled. Theoretically, the tapered distributed amplifier eliminates the reverse waves on the drain lines, and has a class *A* efficiency approaching 50% (Chen & Wang, 2006). Moreover, a paper (Ayasli, Mozzi et al., 1982) proposes to increase the already high gain bandwidth of the TWA by sizing each *T*-section (if the transmission line is to be simplified using a low pass *LCL* filter) *K* times smaller than the previous. Therefore, as reported, the signals travels down the lines toward the load-end, the cutoff frequency becomes *K* times larger and attenuation becomes *K* times smaller from each stage to the next stage. This results in an approximately exponential improvement in bandwidth for the proposed circuit compared to the conventional TWA using same number of stages. However, the gain of each stage is decreasing almost linearly for each stage to the next.

Another paper (Lu, Chen & Lin, 2005) reported a 5-segment non-uniform TWA design with a center segment (3$^{\mathrm{rd}}$ segment) size is adopted and is 2.5 times larger than other segments to boost the transconductance while the others are designed for the required cutoff frequency of the synthetic lines. The reported

pass-band gain of 9.5 dB over a 3 dB bandwidth of 32 GHz in 0.18 μm CMOS process.

A paper (Mesgari et al., 2014) reported a technique of improving noise figure (*NF*) and enhancing gain without consuming additional power. The proposed topology is based on adding a common gate (CG) transistor at the input transmission line for impedance matching with a transconductance of the transistor equal to Z_0. One significant feature of the proposed network is that the noise contribution of the matching CG transistor appears at its source and drain with 180 degrees phase shift while the signal appears with the same polarity at these nodes. This feature is employed in the proposed topology to reduce the noise contribution of the CG matching element as well as increase the gain. The results of the proposed architecture show an average *NF* of 1.8 dB and a gain of 16 dB in a bandwidth of 12 GHz in 0.18 μm CMOS technology.

A conventional TWA reported in (Chang & Lin, 2012) proposed a gate transmission line termination circuit to reduce *NF*. The adopted *RLC* terminal network can reduce the *NF* to a flat and low level over the whole low-to-medium frequency range of DC–7 GHz at an expense of little input matching S_{11} degradation. As a result, S_{11} in the range of 5–17.7 dB, S_{21} of 10.5±1.4 dB, and *NF* in the range of 3.2±0.3 dB were achieved over the DC–10.5 GHz band.

Usually TWA utilizes a single-stage design, but several papers propose different combinations, including parallel (Ayasli, Reynolds et al., 1984), cascaded single-stage (CSSDA) (Tarar et al., 2015), multistage, matrix (Kao & Chen et al., 2013) and even a distributed Doherty amplifier (Lee, Lee, Kam et al., 2009; Cho & Kim et al., 2007).

An interesting approach of increasing the efficiency without compromising bandwidth has been proposed in (Hsiao et al., 2013). The latter paper demonstrated a transmission a gate-drain transmission line folded design approach, which also acted as a transformer. As a result, a well-controlled coupling coefficient was achieved. The paper demonstrated two designs, one in 0.18 μm and the other in 90 nm CMOS process. With the respective gains of 9.5 dB and 7 dB, the TWAs had a bandwidth of 32 GHz and 61.3 GHz with a power dissipation of 71 mW and 60 mW.

A summary of papers reporting TWA research results and parameter improvement solutions in CMOS process is presented in Table 1.5. The reported TWA topologies can be divided into two main groups: conventional and CSSDA. CSSDA topology reports the highest bandwidths of up to 30 GHz in micro-scale processes and up to 80 GHz in nano-scale processes. The TWA is the only advanced PA architecture (comparing to the analysis of ET/EER, DPA and outphasing architectures in this dissertation), which clearly emphasizes an increase in one or several of its parameters (in this case the bandwidth) when shifting to smaller CMOS process scale. Moreover, CMOS TWAs are on par with

III-V semiconductor based ones bandwidth-wise and this makes CMOS even more attractive in the design of low power (femto-, pico- and nano-cells) cells and might push small scale CMOS process development to be even more affordable. Although at the same time, reported TWA papers concentrate on increasing bandwidth and pay less attention to increasing *PAE*. This sets the TWA *PAE* at a level, which is directly dependent upon the biasing class of each segment.The results presented in Table 1.5 can be summarized with the following statements:

1. CMOS TWAs, independently of the process scale, can exhibit bandwidths of tens of gigahertz;
2. CSSDA architecture is reported to achieve higher bandwidths compared to the conventional TWA;
3. TWA concept can be used in both high power (not analyzed in Table 1.5) and low power solutions therefore is suitable for modern wireless equipment.

Main features of the DPA are summarized in the below statements.

TWA architecture advantages:

1. Very high bandwidth. TWA architecture provides an unprecedented bandwidth comparing all other advanced architectures;
2. Can be implemented in both discrete form and integrated into an ASIC. The unmatched bandwidth of the TWA is achieved using both discrete components, a combination of discrete components and PCB microstrips as well as integrated into an ASIC;
3. The achievable bandwidth in CMOS is comparable to that of the designed in *III-V* group semiconductors. Reported CMOS, *SiGe* and *GaAs*/*GaN* BiCMOS TWAs can achieve a similar bandwidth, although power wise *III-V* group semiconductors are more superior;
4. Linearization and predistortion possible. DPD algorithms can be used to extend the linearity of the whole TWA as well as linearizer diodes at the gate of each segment can be placed;
5. *Concept simplicity.* TWA concept is based on transmission line theory, which has matured and is thoroughly investigated;
6. No additional impedance matching network. Due to the innate transmission line impedance of 50 Ω, there is no need to include impedance matching networks;

7. A choice of different architecture variations. Single-stage, multi-stage, parallel, matrix in both uniform and non-uniform arrangement are at the disposal of the designer.

Table 1.5. Summary of reviewed traveling wave amplifiers in CMOS process

Ref.	Process	*VDD*, V	Δ*f*, GHz	A_v, dB	*NF*, dB	Topology
(Huang, Lin, Cheng et al., 2015)	0.18 µm CMOS	2.8	1.5–35.5	25	6.5–8	CSSDA
(Kao & Chen et al., 2013)	0.18 µm CMOS	2.8	DC–35	20.5	6.8–8	CSSDA
(Mesgari et al., 2014)	0.18 µm CMOS	1.8	0.1–12	16	0.9–3.8	Conventional
(Chang & Lin, 2012)	0.18 µm CMOS	1.8	DC–10.5	10.5	3.2	Conventional
(Moez & Elmasry, 2006)	0.18 µm CMOS	1.8	DC–10	15	–	Conventional
(Aguirre et al., 2007)	0.13 µm CMOS	2.4	0.05–32.5	8.8	–	Conventional
(Piccinni, 2016)	0.13 µm CMOS	1.2	3–10	14	1.8–3.3	Conventional
(Ellinger, Sakalas et al., 2008)	90 nm CMOS SOI	2	0.1–25, 0.1–40	10, 8	4.5–9	Conventional
(Hsiao et al., 2013)	90 nm CMOS	2.2, 1.5, 0.66	DC–40	14	6–8	Gate–drain transformer coupling
(Tarar et al., 2015)	65 nm CMOS	–	DC–70	25	5–7.5	LC-CSSDA
(Gertman & Socher, 2013)	65 nm CMOS	2.4	4.7–11.7	12	–	Conventional
(Chen, Yeh et al., 2014)	40 nm digital CMOS	1.7	DC–80	15	–	CSSDA

TWA architecture disadvantages:

1. Large area due to multiple inductors. This makes integration into transceiver chips (ASICs containing not only a single PA) very difficult and impractical if not impossible;
2. Efficiency of basic PA classes. TWA has an outstanding bandwidth, but the *PAE* is naturally decreasing with the increase of the frequency. The architecture itself is not aimed at improving the *PAE*;
3. Additional noise due to source and drain termination resistors. The latter noise can be reduced by integrating reported termination noise reduction techniques.

1.1.8. Millimeter Wave Radio Frequency Power Amplifier

Millimeter wave RF PAs are intended to work at frequencies above 25 GHz, which corresponds to the high-band 5G range. The published papers related to mm-wave PA research reveal an overall tendency of architectures which are used in frequency ranges above 25 GHz. Papers (Indirayanti & Reynaert, 2017; Li & Wang, 2018; Hamed et al., 2018) present detailed mm-wave CMOS PA reviews distinguishing architecture types alongside their research results. According to the review tables in the latter papers, advanced PA architectures, such as DPA, ET/EER PA, TWA or outphasing PA, are rarely implemented at frequencies above 25 GHz in CMOS process node. The most common architectures in the mm-wave range are single- or two- stage stacked approaches in both single-ended and differential forms and often operate in nonlinear regions (ex. class-*E*, class-*F*). Papers (Ali et al., 2019; Li & Wang, 2018; Hamed et al., 2018) propose mm-wave DPAs although nanometer CMOS processes (ex. 45 nm, 28 nm) are utilized. Concluding the results presented in the above papers, complex architecture solutions (such as envelope tracking) are irrelevant in mm-wave PAs and are usually kept as simple as possible, close to the classic arrangement. Moreover, according to (Rostomyan et al., 2018; Pham et al., 2017) high-efficiency mm-wave PAs designed using silicon on insulator (SOI), Gallium Arsenide pseudomorphic high electron mobility transistors (*GaAs* pHEMT), Silicon Germanium heterojunction bipolar transistors (*SiGe* HBT's) or Gallium Nitride (*GaN*) processes provide superior performance compared to CMOS. Due to the fact, that a small number of different architecture solutions in CMOS has been published, mm-wave PAs are not further elaborated in this dissertation.

1.1.9. Comparison of Power Amplifier Architectures

A summary of advanced CMOS PA architectures discussed in Chapter 1.1.3 through Chapter 1.1.6 is presented in Table 1.6. A classical linear CMOS PA is also included as it is the main building block for the other advanced and intricate topologies. The latter table is organized in a way to compare all discussed architectures by means of emphasizing the main achievable specifications and features in submicron CMOS process, as well as pointing out the existing restrictions. Millimeter-wave power amplifiers are not included in the latter table as the utilized architectures are usually variations of classical PA, DPA or TWA configurations.

Table 1.6. Summary of the reviewed advanced power amplifier architectures in CMOS

Classic linear CMOS PA	CMOS DPA	CMOS ET/EER PA	CMOS Outphasing PA	CMOS TWA/DA
Process(es) and supply voltage reported to exhibit highest *PAE*				
–	0.13–0.18 μm, V_{DD} = 3.3 V	0.15–0.32 μm, V_{DD} = 3.3 V	Dependent on the DSP algorithms and wireless standard.	–
$PAE_{average}$, P_{in}=[$P_{back\text{-}off}$…P_{1dB}]				
5–30%	20–45%	17–48%	20–60%	Same as classic linear
V_{DD} range				
2–5.5 V	2.5–5.5 V	2–5 V	1.8–3.6 V	0.66–2.8 V
Operating bandwidth				
≤500 MHz. Can be widened introducing negative feedback.	≤500 MHz. Can be increased up to 1 GHz introducing an alternative output impedance inverter.	≤40 MHz. The supply regulator forms a bottleneck.	≤40 MHz. The power combiner forms a bottleneck.	≥5 GHz
Architecture features				
Is the basis for all advanced architectures.	Average *PAE* doesn‘t deviate from highest value at input signal power back-off of 5–8 dB; Different architecture variations available.	Different architecture variations available; *PAE* improvements of up to 20% possible; Linearization and predistortion possible but difficult.	Very high *PAE* due to utilizing nonlinear PAs to form a linear signal; Predistortion possible; Efficiency can be increased without hardware changes.	Different architecture variations available; Linearization and predistortion possible; No additional IMN; Bandwidth comparable to that of *III-V* based PAs.
Circuit blocks utilized by architecture				
Active device, feedback and linearization components (optional), impedance matching networks.	Main and auxiliary PAs, impedance matching networks, power splitter, impedance inverter.	PA, impedance matching network, supply modulator.	Two nonlinear or linear PAs in parallel, impedance matching network, power combiner, SCS.	Multiple identical/different PA sections and termination resistors.

Table 1.6. continued

Classic linear CMOS PA	CMOS DPA	CMOS ET/EER PA	CMOS Outphasing PA	CMOS TWA/DA
Potential of integrating in a single ASIC and/or implementing in portable wireless devices				
All components can be integrated in a single dedicated ASIC as well as in a multifunc-tional transceiver.	All components can be integrated in a single dedicated ASIC. Integration in multifunctional transceiver very difficult and impractical if not impossible. The integration bottleneck is the power combiner.	All components can be integrated in a single dedicated ASIC except the DC-DC regulator (if included) power inductor. Integration in a multifunctional transceiver very difficult and impractical if not impossible.	All components can be integrated in a single dedicated ASIC. Integration in multifunctional transceiver very difficult and impractical if not impossible. The integration bottleneck is the power combiner.	All components can be integrated in a single dedicated ASIC. Integration in multifunctional transceiver very difficult and impractical if not impossible.
Main restrictions				
Potential for linearity, *PAE* and bandwidth improve-ments.	Large area due to input power splitter and output imped-ance inverter; Bandwidth limited by out-put impedance inverter.	Overall system complexity; Addi-tional noise if switching regulator used; Sup-ply modulator de-fines narrow bandwidth.	Specific phase compensated power combiner required, which also restricts the bandwidth.	Large chip area due to multiple inductors; Additional noise from termination resistors; No significant *PAE* improvements.

The results resented in the below summary are used during the formulation of the dissertation problem in Chapter 1.3.

1.2. Impedance Matching Network Synthesis Algorithms and Possible Vectors for Improvement

Impedance matching is essential to any high frequency amplifier, including the LNA and PA, to operate at its maximum gain and efficiency minimizing noise. This chapter presents different impedance matching methodologies that are in use as well as their capabilities and restrictions.

1.2.1. Concept of Impedance Matching

Impedance matching is a procedure of equalizing the source and load circuit impedances for the highest power transfer – the load impedance Z_L must be a complex conjugate of the source impedance Z_S. Complex conjugate simply refers to a complex impedance having the same real part with an opposite reactance value. Thus, if the source impedance were $Z_S = R_S + jX_S$, then its complex conjugate would be $Z_S = R_S - jX_S$ (Bowick, 2007). It is not possible to match an arbitrary impedance even to a pure resistance over the whole frequency spectrum, or even at all frequencies within a finite frequency band. Hence, for any RF amplifier, impedance matching network should provide matching over the complete frequency band of interest. On the other hand, it is possible to obtain a match at any desired number of frequencies, provided the given impedance has a finite resistive component at those frequencies. Such a matching, however, has little practical value because it is incorrect to assume that one can obtain a reasonable match over a frequency band by correctly matching at a sufficiently large number of frequencies within the desired band. The following results in the statement that any matching problem must include the maximum tolerance on the quality of the match as well as the minimum bandwidth within which the match is to be obtained (Mhala, Desai & Kuma, 2008; Fano, 1948).

1.2.2. Existing Impedance Matching Methods and Techniques

Impedance matching networks can be divided into narrowband and wideband groups implemented using lumped, distributed or mixed (lumped-distributed) components. The latter types of impedance matching networks, as well as variable network variants, are described in this subsection.

Narrowband. Generally a circuit is defined as narrowband when the relative passband of less than 15% (Li, 2012). Load and source impedances in general case are complex, having a real and imaginary parts. The two basic approaches in handling complex impedances are absorption and resonance. The simplest and most widely used matching circuit is the *L*-type network, which contains two components. The latter type of network has a constant *Q*-factor which is directly dependent on source and load impedances, thus can't be changed. As a result, the circuit has lower versatility but its design is simple and straightforward.

Three element networks, π-type and *T*-type, provide more flexibility in matching the source and the load as the *Q*-factor can be defined making the bandwidth as narrow as desired (Orfanidis, 2016). The latter networks are presented in Fig. 1.19. The π- and *T*-type networks can be transformed into each other by the following standard impedance transformations, which are cyclic permutations of each other (Orfanidis, 2016).

$$Z_a = \frac{Z_2 Z_3}{U},\ Z_b = \frac{Z_1 Z_3}{U},\ Z_c = \frac{Z_1 Z_2}{U},\ U = Z_1 + Z_2 + Z_3, \tag{1.34}$$

$$Z_1 = \frac{V}{Z_a},\ Z_2 = \frac{V}{Z_b},\ Z_3 = \frac{V}{Z_c},\ V = Z_a Z_b + Z_b Z_c + Z_c Z_a. \tag{1.35}$$

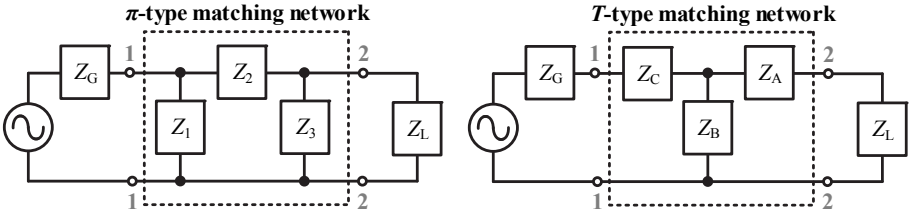


Fig. 1.19. All possible π- and T-type matching network configurations

A different approach based on calculating two "back-to-back" L-type networks to form a π-type or "flip-flopped" L-type networks to form a T-type. In both cases a virtual resistor is used to connect the two L-type networks. Two L-type networks have a total of four components therefore one might leave all of them to form the final π-type or L-type network, or merge the ones that are in parallel or in series. This simplifies the component number in the network to three (Bowick, 2007).

In order for the π-type or T-type network to always have a solution, a minimum Q-factor condition must be satisfied (Orfanidis, 2016) according to

$$Q_{\min} = \sqrt{\frac{R_{\max}}{R_{\min}} - 1}. \tag{1.36}$$

Sources (Bowick, 2007; Grebennikov, 2012; Orfanidis, 2016; Шварц, 1980), provide methods of calculating two and three component matching and RF bias networks. A generalized summary of impedance matching conditions and existing number of solutions is presented in Table 1.7.

Table 1.7. Summary of impedance matching conditions

Matching conditions	Number of possible L-type networks	Number of possible π-type networks	Number of possible T-type networks
$R_G > R_L$, $\lvert X_L\rvert \geq [R_L(R_G - R_L)]^{1/2}$	2 forward and 2 reversed networks	4*	4*
$R_G > R_L$, $\lvert X_L\rvert < [R_L(R_G - R_L)]^{1/2}$	2 forward networks	4*	4*
$R_G < R_L$, $\lvert X_G\rvert \geq [R_G(R_L - R_G)]^{1/2}$	2 forward and 2 reversed networks	4*	4*
$R_G < R_L$, $\lvert X_G\rvert < [R_G(R_L - R_G)]^{1/2}$	2 forward networks	4*	4*

* with the condition of satisfying the minimum Q-factor

Wideband. Generally a circuit is defined as wideband when the relative pass-band of more than 15% (Li, 2012).The design for a broadband matching circuit solve a problem with contradictory requirements: wider matching bandwidth with minimum reflection coefficient $\Gamma(\omega)$, or how to minimize the number of the matching network sections for a given wideband specification. The necessary requirements are determined by the Bode-Fano criterion, which provide a theoretical limit on the minimum reflection coefficient magnitude for certain canonical types of load impedances that can be obtained with an arbitrary matching network.

So, for the lossless network with a parallel *RC* load impedance shown in Fig. 1.20a and with a series *LR* load impedance shown in Fig. 1.20b the Bode-Fano criterion states that

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} d\omega \le \frac{\pi}{\tau}, \tag{1.37}$$

where $\tau=RC=L/R$, $\Gamma(\omega)$ is the reflection coefficient seen looking into the arbitrary lossless matching network.

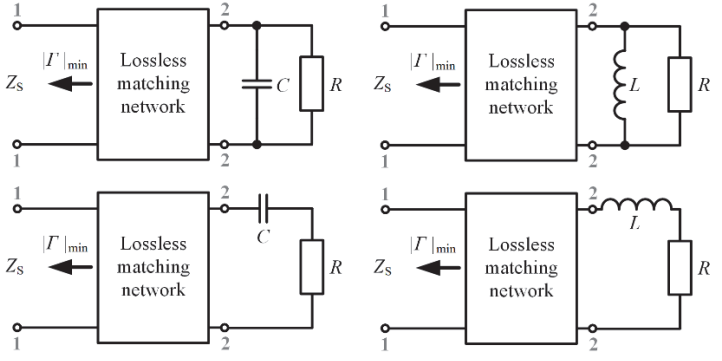


Fig. 1.20. Variations of loaded lossless matching circuits described by Bode-Fano integrals: (a) parallel and series *RC*; (b) parallel and series *RL*

For the lossless network with a series *RC* load impedance shown in Fig. 1.20a and with a parallel *RL* load impedance shown in Fig. 1.20b, the Bode-Fano integral is defined as

$$\int_0^\infty \omega^{-2} \ln \frac{1}{|\Gamma(\omega)|} d\omega \le \pi\tau . \tag{1.38}$$

The mathematical relationship expressed by Eq. (1.37) or Eq. (1.38) is shown in Fig. 1.21 – the two plots reflect an ideal filter with a flat response over the required frequency bandwidth. Both plots illustrate an important tradeoff for the

same load: the wider the matching network bandwidth, the worse the reflection coefficient magnitude.

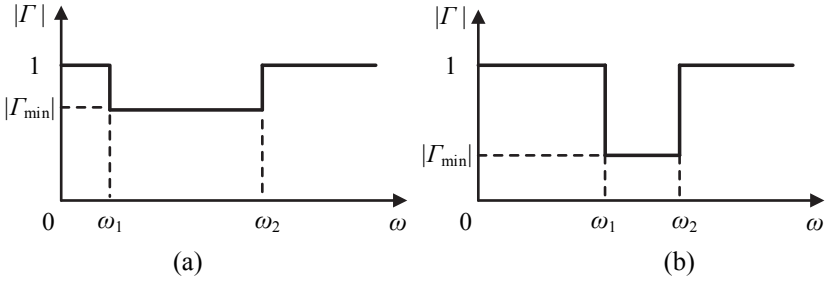


Fig. 1.21. Ideal filter flat response, described by Bode-Fano integrals

For a given frequency bandwidth $\Delta\omega = \omega_2 - \omega_1$ the minimum reflection coefficient can be derived as

$$\left|\Gamma\right|_{\min} = \exp\left(\frac{-\pi}{\Delta\omega\tau}\right). \tag{1.39}$$

It should be noted that the theoretical bandwidth limits can be realized only with an in finite number of matching network sections. Moreover, the frequency bandwidth with minimum reflection coefficient magnitude is determined by a loaded quality factor $Q_L = \omega_0\tau$ for the series *RL* or parallel *RC* circuit and $Q_L = 1/\omega_0\tau$ for the parallel *RL* or series *RC* circuits.

When designing broadband matching circuits for power amplifiers it is necessary to transform and match the device complex impedances with the source and load impedances, which are usually resistive and equal to 50 Ω. For high-power or low-supply voltage cases, the device impedances may be small enough, and it needs to include an ideal transformer (IT) together with a matching circuit, as shown in Fig. 1.22. Such an ideal transformer provides only a transformation between the resistances applied to its input and output and does not have any effect on the circuit frequency characteristics.

Norton transformation is applied to implement an ideal transformer by means of an equivalent capacitive or inductive circuit as shown in Fig. 1.23. An ideal transformer with an *L*-type capacitor configuration (Fig. 1.23a) can be replaced by an equivalent π-transformer C_{I}, C_{II} and C_{III} (Fig. 1.23b) with the following values

$$C_{\text{I}} = n_{\text{T}}(n_{\text{T}} - 1)C_1,\ C_{\text{II}} = n_{\text{T}}C_1,\ C_{\text{III}} = C_2 - (n_{\text{T}} - 1)C_1, \tag{1.40}$$

where n_{T} is the transformation coefficient. In this case, all of the parameters for these two-port networks are identical at any given frequency. However, such a replacement is possible only if the capacitance C_{III} is positive and, consequently, physically realizable.

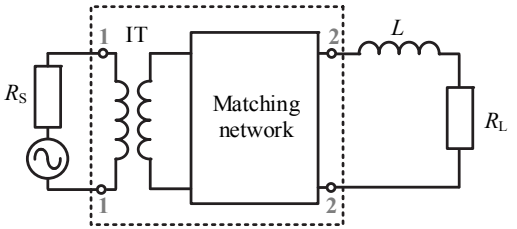


Fig. 1.22. Matching circuit with ideal transformer

An ideal transformer with an *L*-type inductor configuration (Fig. 1.23c) can be replaced by an equivalent π-transformer $L_{\rm I}$, $L_{\rm II}$ and $L_{\rm III}$ (Fig. 1.23d) with the following values

$$L_{\rm I} = n_{\rm T}(n_{\rm T} - 1)L_2\,,\ L_{\rm II} = n_{\rm T}C_2\,,\ L_{\rm III} = L_1 - (n_{\rm T} - 1)L_2\,. \qquad (1.41)$$

The replacement is possible only if the inductance $L_{\rm III}$ defined is positive and, consequently, physically realizable. Other Norton transformers and their equivalents are discussed in (Хотунцев, 1978).

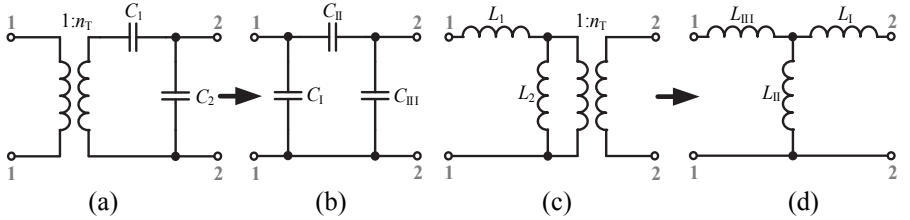


Fig. 1.23. Matching network transformations: (a, b) capacitive and (c, d) inductive Norton transformation circuits

One of the design methods for such matching circuits is based on the theory of transforming ladder configuration low-pass filters containing series inductances alternating with shunt capacitances (Grebennikov, 2012; Bowick, 2007). The maximum passband ripples and coefficients are calculated using two-section low-pass Chebyshev filter design coefficients. Another approach is based on transforming the low-pass prototype filters, whose simple *L*-, *T*- and π-type circuits, to the bandpass filters. The transformation from the low-pass to bandpass prototype filters can be obtained using frequency substitution in the form of

$$\omega \to \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right), \qquad (1.42)$$

where $\omega_0 = \sqrt{\omega_1\omega_2}$, $\Delta\omega = \omega_2 - \omega_1$, $\omega = 2(f_2 - f_1)/(f_2 + f_1)$ and $\omega_1 = 2\pi f_1$, $\omega_2 = 2\pi f_2$ being the low and high edges of the passband. As a result, a series inductance $L_{\rm k}$ can be transformed into a series *LC* circuit according to

$$\omega L_k = \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)L_k = \omega\frac{L_k}{\Delta\omega} - \left(\frac{\omega\Delta\omega}{\omega_0^2 L_k}\right)^{-1}. \quad (1.43)$$

Similarly, a shunt capacitance C_k is transformed into a shunt LC circuit based on

$$\omega C_k = \frac{\omega_0}{\Delta\omega}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)C_k = \omega\frac{\Delta\omega}{C_k} - \left(\frac{\omega\Delta\omega}{\omega_0^2 C_k}\right)^{-1}. \quad (1.44)$$

When designing an interstage impedance-transforming circuit, it is necessary to take into account the parasitic capacitance and inductance of the device output, together with the parasitic inductance of the device input, but the design procedure is the same as with a purely resistive load.

An approach to designing wideband impedance matching network for purely resistive source and load is to use "forward" or "reverse" L-type network ladders with virtual resistors. A three segment "reverse" L-type network is presented in Fig. 1.24. In this case, the Q-factor of each successive segment depends on the ratio of resistances on the ends of each segment. The maximum bandwidth (minimum Q) available from this network is obtained when the virtual resistor (R_{virt}) is made equal to the geometric mean of the two impedances being matched and can be expressed as

$$R_{\text{virt}} = \sqrt{R_{\text{S}} R_{\text{L}}}. \quad (1.45)$$

The loaded Q-factor of the network is defined as

$$Q = \sqrt{\frac{R_{\text{virt}}}{R_{\text{smaller}}} - 1} = \sqrt{\frac{R_{\text{larger}}}{R_{\text{virt}}} - 1}, \quad (1.46)$$

where R_{smaller} is the smallest terminating resistor and R_{larger} is the largest termination resistor.

The approach presented in Fig. 1.24 can be extended by cascading more stages with the optimal bandwidths obtained by the following ratios of the resistors on each end of a single stage

$$\frac{R_{\text{virt1}}}{R_{\text{smaller}}} = \frac{R_{\text{virt2}}}{R_{\text{virt1}}} = \frac{R_{\text{virt3}}}{R_{\text{virt2}}} = \ldots = \frac{R_{\text{larger}}}{R_{\text{virt}n}}. \quad (1.47)$$

In practice, more than three matching stages are considered impractical due to the increased losses in the network itself (Bowick, 2007).

Lumped. Both narrowband and wideband matching networks, described above, can be implemented using discrete capacitors and inductors. Due to innate component parasitics (*ESR*, lead inductance, leakage resistance, parasitic capacitance), their frequency responses doesn't exactly follow those of ideal components therefore calculated ideal component values have to be tweaked when using lumped components.

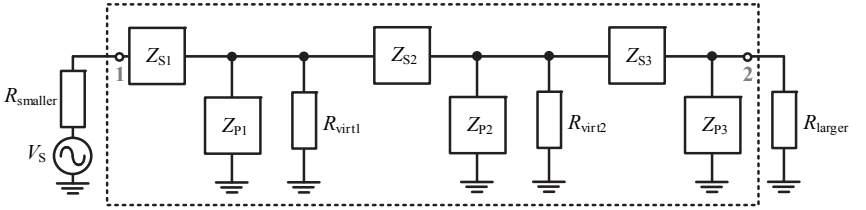


Fig. 1.24. Three-segment "reverse" *L*-type matching network with virtual resistors

Moreover, both capacitors and inductors have *ESR* and self-resonant frequencies (*SRF*), which differ from component to component. The latter have to be included as they reduce the overall *Q*-factor of the network.

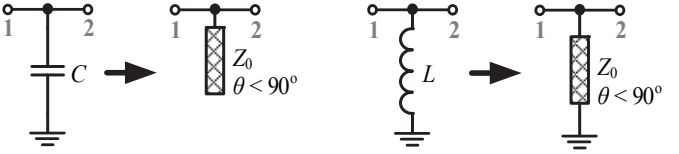


Fig. 1.25. Lumped and distributed component single frequency equivalence

Distributed. Impedance matching between source and load can be done utilizing distributed parameter components – transmission line elements. The input impedance of transmission line configurations at a particular frequency can be expressed as that of a lumped element and is shown in Fig. 1.25. The equivalent inductance and capacitance at a frequency ω is calculated from

$$L = \frac{Z_0 \tan\theta}{\omega}, \theta < \pi / 2, \tag{1.48}$$

$$C = \frac{\tan\theta}{\omega Z_0}, \theta < \pi / 2. \tag{1.49}$$

The converted components can be implemented in *L*-, *T*- and π-type circuits identical to those shown in Fig. 1.19. Due to the small achievable capacitance, distributed capacitors are not as widely used as distributed inductors. Small value distributed inductors, on the other hand, can be precisely calculated, have a smaller *ESR* and are more stable (much higher self-resonant frequency) comparing to the lumped ones (Grebennikov, 2012; Mhala, Desai & Kuma, 2008). The simplest way of matching the source and the load is to use a quarter-wave transmission line with an optimal impedance of

$$Z_{\lambda/4} = \sqrt{Z_S Z_L}. \tag{1.50}$$

The latter method provides sufficient matching, but is limited by the bandwidth due to the distributed component impedance shifting proportionally to the $1/\omega$ (Eq. 1.48 and Eq. 1.49) and not sufficing the optimal value given by

Eq. (1.50). A broader bandwidth can be obtained by connecting multiple $\lambda/4$ lines with different impedances in series. Moreover, the latter different impedance transmission line segments can be connected in a step configuration or using a taper.

Two other possible methods of matching a complex load are to use a shorted or open stub connected in parallel with the load, and adjusting its length or its line impedance so that its susceptance cancels the load susceptance. This results in a real load that can then be matched by the $\lambda/4$ section. In the first method, the stub length is chosen to be either $\lambda/8$ or $3\lambda/8$ and its impedance is determined in order to provide the required cancellation of susceptance. In the second method, the stub's characteristic impedance is chosen to have a convenient value and its length is determined in order to provide the susceptance cancellation. In practice, both methods are mostly used with microstrip lines that have easily adjustable impedances. Other stub matching methods include single stub, balanced stubs, multi-stub (Grebennikov, 2012).

One major disadvantage of distributed matching networks compared to lumped ones is the large required PCB space. The space can be partially reduced by utilizing materials with larger than standard values of dielectric permittivity $\varepsilon_r = [3\ldots5]$, such as ceramics ($\varepsilon_r \sim 10$). However, this increases the solution price and requires special handling during manufacturing and application.

Mixed. A more common method of matching is utilizing both lumped and distributed approaches at the same time. An example of such a circuit can be the inclusion of the innate inductance of a 50 Ω feedline into the component values of a distributed matching network or adding stubs for frequency tuning (FitzPatrick, 2017). The advantage of using a combination of distributed and lumped components is the precision and a possibility of fine-tuning the network response with a reasonable occupied PCB space.

Other reported matching methods and configurations. One of the simplest ways of matching an amplifier in a broad range of frequencies is to design different matching networks for different frequencies and then switch between the bands using two single-pole *N*-throw switches. This is probably the simplest method and can be equally adapted to both lumped and distributed networks, but it requires large PCB area, especially in the case of distributed ones. Moreover, switch isolation might become an issue at the input and power handling capability – at the output of a PA. Therefore, different approaches on creating reconfigurable impedance matching networks have been reported.

A paper (Added & Boulejfen, 2015) reports adopting a "*CLC*" π-type matching network for the purpose of making it variable. The capacitors in the network are implemented as varactor diodes. The proposed variable impedance matching network operates at 2.4 GHz and can cover a broad range of loads. The matching reflection coefficient S_{11} reaches a value as low as −25 dB in the entire

impedance coverage. The proposed network is intended for narrow-band applications but can be integrated in multiband applications. Another paper (Rosolowski et al., 2010) also reports using varactor-controlled matching networks with the intention of increasing bandwidth, rather than covering a broad range of loads. The achieved bandwidth spans from 1.3 GHz to 2.6 GHz in steps of 100–300 MHz. A paper (Sanchez-Perez et al., 2011) proposes an analysis of utilizing a reconfigurable matching network based on a varactor diode. The design aim is to provide both bandwidth and a wide range of loads. The reported matching network covers at least 40% of the Smith chart in the frequency range of 300 MHz to 850 MHz. The Smith chart coverage reaches 90% and more in the range of 600 MHz to 850 MHz.

A paper (Yuan & Suzuki, 2016) reports a method of calculating impedance matching networks including lumped component ohmic loss. The proposed approach has been confirmed effective for any two different impedance pairs to be conjugated matched. A paper (Sanchez-Perez et al., 2010) proposes the use of a micro-electro-mechanical system (MEMS) switch-based reconfigurable matching network to improve the linearity and efficiency of an RF power amplifier under load variations. It is based on reactive lumped elements, namely series inductors and switched capacitors in a "*CCLCCLCCLCC*" configuration, where *L* indicates the presence of a series inductor and *C* the appearance of a shunted capacitor in series with a single-pole single-throw MEMS switch. On average, more than 10 dB *ACPR* increase and 4% efficiency increase can be achieved when working at maximum output power of 37 dBm. The design has been optimized to ensure a correct operation in the 300–700 MHz range. A summary of existing impedance matching methods and circuit configurations is presented in Table 1.8. A dual-band matching network is reported in (Maktoomi et al., 2014) paper. The design utilizes a dual-band (folded) $\lambda/4$ section, a stub and a series TLine section. The reported methodology can be used to design any dual-band matching network and the paper presented 1 GHz and 2 GHz network, with $S_{11} \leq -10$ dB.

Smith chart. The methods of calculating impedance matching networks discussed above are analytical and sometimes complicated. Smith chart is one of the tools most widely used to match circuit designs because it provides a graphical representation of the consecutive matching design procedure and can be applied to both lumped elements and transmission lines. Moreover, there are impedance and admittance Smith charts so it is possible to graphically solve for a matching network when dealing with both impedances and admittances.

Table 1.8. Summary of impedance matching methods and circuits

Advantages	Disadvantages
Lumped	
• Small occupied PCB area; • Can provide a wider bandwidth compared to distributed due to innate parasitics; • Can fixed or variable; • Can be integrated into system in package (SiP).	• Restricted by commonly manufactured component values; • Innate parasitics can cause stability issues; • Calculated ideal component value has to be fine-tuned due to innate parasitics; • Frequency tuning can only be done by optimizing component values; • Larger losses in network due to innate component parasitics; • Cannot be integrated into ASICs.
Distributed	
• Can be fixed or variable; • Frequency tuning can be done by means of connecting pre-deposited stubs; • Small value inductors and capacitors can be precisely calculated; • No extra cost for matching network components and PCB assembly; • Smaller losses in network due to neglectable component parasitics; • Are integrated into ASICs and can be integrated in SiP at high frequencies (≥5 GHz).	• Large occupied PCB area; • Large value capacitors and inductors are not physically realizable; • Might require additional cost for high quality dielectric and/or impedance control for precise operation in the gigahertz range.
Mixed	
• Can be fixed or variable; • Lumped components are used as large value elements, whereas the small value ones are precise low loss dis-tributed components; • Occupies less space than purely distributed, but more space than lumped; • Can be integrated in SiP at high frequencies (≥5 GHz).	• Might require additional cost for high quality dielectric and/or impedance control for precise operation in the gigahertz range.

Other parameters that are very important to any RF circuit, such as voltage standing wave ratio (VSWR), reflection coefficient or losses in the matching network, can also be graphically determined.

1.3. First Chapter Conclusions and Dissertation Problem Formulation

The analysis presented in first three Chapter 1 sections can be summarized with the following concluding statements:

1. Modern wireless systems comprise of different output power and number of user supporting radio access nodes and shift from a traditional to heterogeneous architecture. Heterogeneous elements are divided into different transmit power cells. From an architectural point of view, macro-cell and femto-cell transceivers are usually identical and are comprised of the same RF circuit blocks. Macro-cells cope with high power (up to hundreds of watts) RF signals, which typically require the PAs to be implemented using *III-V* group semiconductors and are usually stationary. Even though wireless transceivers can be fully implemented using *III-V* group semiconductors, a low level of integration and small digital capabilities (the lack of a proper integrated DSP, self-calibration capabilities, etc.) lead to a high price to functionality ratio, hence are not suitable for portable low power cells. CMOS, on the other hand, is scalable and provides a high level of integration for both analog and digital circuits at a reasonable (compared to that of *III-V* group semiconductors) price. Due to low breakdown voltage, CMOS is not suitable for high power applications, but is perfect for low power transceiver blocks, including low power RF PAs.
2. Classical linear RF PA architecture exhibits high levels of linearity but lacks efficiency (5–20%). Due to the reported increase in modern wireless network capacity, RF PAs with higher levels of efficiency without sacrificing linearity are required. The most promising PA architectures for low power cells are reported to be ET/EER, outphasing, DPA and TWA, all of which are suitable to be designed in CMOS process. ET/EER PA can reach operating bandwidths of up to 40 MHz with an efficiency of 17–48%, but has a high level of complexity and additional noise injected from the supply modulator. The outphasing architecture provides bandwidths of up to 40 MHz with an efficiency of 20–60%, but has low potential of increasing the bandwidth. DPA architecture provides bandwidths of up to 500 MHz with efficiency of 20–45% and has an inherent back-off power region, where the efficiency doesn't deviate from its highest value. The downside of the DPA architecture is its limitations due to the output impedance inverter. TWA provides an outstanding bandwidth of up to 80 GHz and is the only advanced PA architecture that is comparable to that of *III-V* group semiconductor PAs.

Nevertheless, its disadvantages are the large number of inductors (usually more than 4) which increases the occupied area and no improvements in efficiency compared to that of basic PA classes. It has also been observed, that CMOS scaling doesn't always lead to an increase in low power RF PA parameters and PAs implemented in submicron 0.13–0.18 μm CMOS processes exhibit the highest gain, efficiency and bandwidth (published 0,35 μm – 28 nm CMOS PA have been reviewed).

3. Most of the reported advanced RF PA architectures are suitable to undergo linearization using the currently promising adaptive DPD and other predistortion techniques.

4. Reported impedance matching techniques provide different fixed and variable distributed, lumped and mixed solutions that can be employed in modern wireless systems. Due to the fact that component parasitics in the RF transmission chain can alter the arbitrary load impedance seen by the source, a method of utilizing varactor diode based reconfigurable matching network when the design aim is to provide both bandwidth and a wide range of loads seems very promising. Due to the high versatility and small occupied area of lumped matching networks are common in modern wireless systems, so a methodology of including lumped component ohmic loss has also been reported. Other reported matching networks employ different solid-state and MEMS switches to create reconfigurable matching networks.

The above conclusions lead to the following tasks that form the dissertation problem:

1. An RF PA architecture with impedance matching networks suitable for low- to mid-power (up to 24 dBm) portable mid-band 5G applications, providing IF bandwidths of more than 150 MHz as well as improved efficiency, compared to the classical PAs, is required. The latter architecture should occupy area that doesn't make integration in a modern agile transceiver impractical must be suitable for employing linearization techniques, such as adaptive DPD.
2. Impedance matching networks are concurrent to any power amplifier. Lumped impedance matching components (capacitors and inductors) have innate parasitics (*ESR*, parasitic inductance and capacitance leading to component *SRF* and leakage resistance all of which differ for various component packages). Neglecting these parasitic parameters results in multiple iterations to fine-tune the final network component values for optimal 5G wireless device operation at the target frequency. Hence, a compensation methodology, which takes into account lumped matching component parasitic parameters is required.

2

Impedance Matching Network Research, Design and Synthesis

Impedance matching is concurrent with any RF circuit design, including the design of RF PAs. Based on the analytical research, presented in Chapter 1.3, vectors of matching network calculation techniques have been selected. The following chapter presents a proposed impedance matching network synthesis (*IMNS*) mathematical model and surface mount component (SMD) package parasitics compensation algorithm in detailed description. The test-bench PCBs, measurement results and conclusions are also included. Research results presented in this chapter address dissertation problem No. 2, raised in Chapter 1 conclusions section – the need for an impedance matching methodology that takes into account lumped matching component parasitic parameters.

The research results presented in this chapter have been included in a *Clarivate Analytics Web of Science* databases referred publication (Vasjanov & Barzdenas 2018, Sep.) with a citation index.

2.1. Proposed Impedance Matching Algorithm

The proposed lumped impedance matching network synthesis (*IMNS*) algorithm is presented in Fig. 2.1. The algorithm is intended to be used as a

compensation technique after the impedance matching networks have been designed using classical matching techniques.

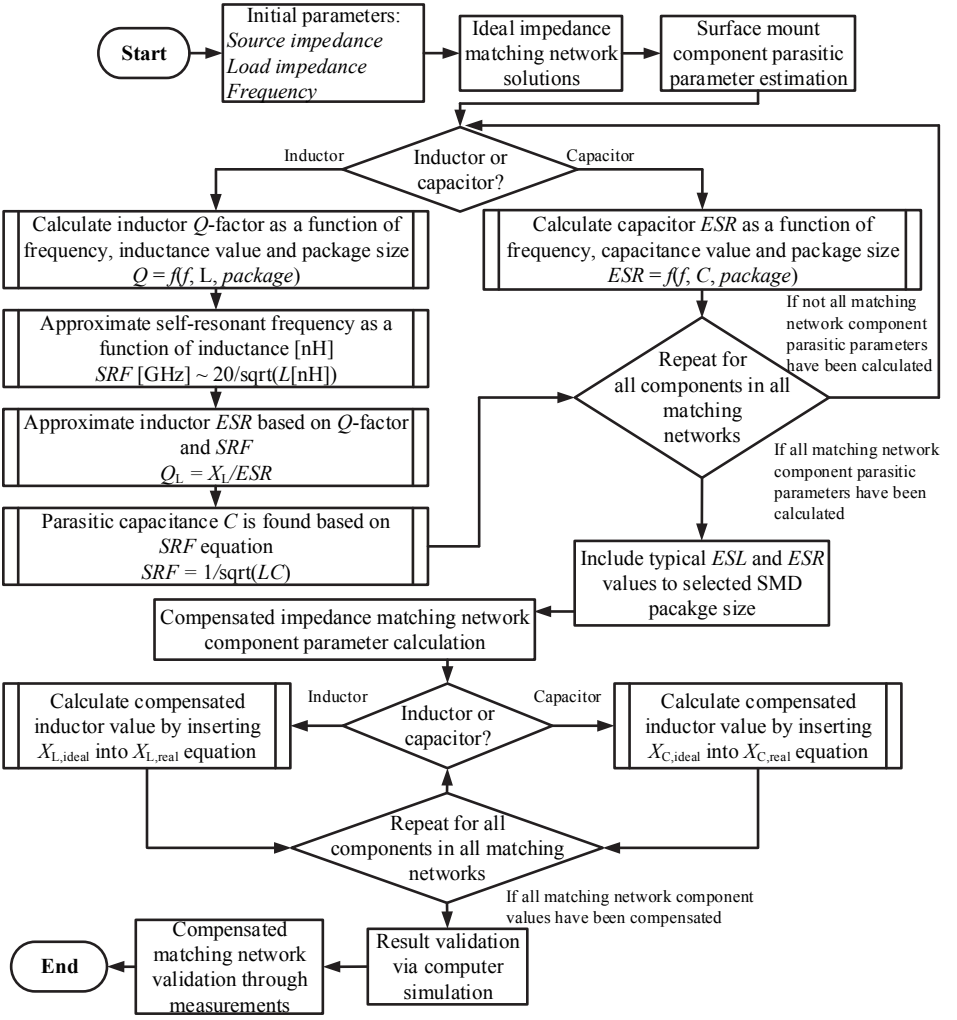


Fig. 2.1. Proposed impedance matching network compensation algorithm

The latter aim has been raised in this dissertation because of the problems encountered in the initial stage of fabricated power amplifier ASIC experimental research. The minimum of the impedance matching S_{11} curve was noticed to be off the target frequency by a certain offset. As a result, several simulation and measurement iterations were required to compensate this offset and match the impedances at the exact target frequency. Thus, a decision was made to conduct

research and improve the methodology of calculating lumped component matching networks.

The proposed algorithm is based on estimating SMD component (capacitor and inductor) parasitics, such as *Q*-factor, *ESR*, *ESL*, *SRF* and leakage resistance, based on the component value (capacitance or inductance), frequency and SMD package size. The need of such a compensation arises from the fact, that the latter parasitic parameters shift the matching response (usually to the lower side of the frequency range) by a certain value. This value is dependent on the center frequency, but can reach several hundreds of megahertz. As a result, with no compensation techniques, the designer can match the network to the desired frequency only via several calculation and measurement cycles.

The proposed *IMNS* algorithm provides compensated matching network component values, which match the source and load impedances at the desired frequency, eliminating the need of fine-tuning the values.

Lumped capacitor and inductor models with their respective parasitic parameters are presented in Fig. 2.2 (Eroglu, 2016). The latter models have been selected as the estimated component parasitic parameters and equations presented in this dissertation have been derived using the data presented by major capacitor and inductor manufacturers.

The lumped inductor model has the following parasitic parameters:

- L_{PKG} – SMD package parasitic inductance, *ESL*;
- R – SMD package series resistance, *ESR*;
- C_S – parasitic capacitance, which, alongside with L, defines *SRF*;
- L – inductance value.

Similarly, the lumped capacitor has the following parasitic parameters:

- L_{PKG} – SMD package parasitic inductance, *ESL*;
- R_S – SMD package series resistance, *ESR*;
- R_d=1/G_d – capacitor parasitic drain resistance (or conductance G_d);
- C – capacitance value.

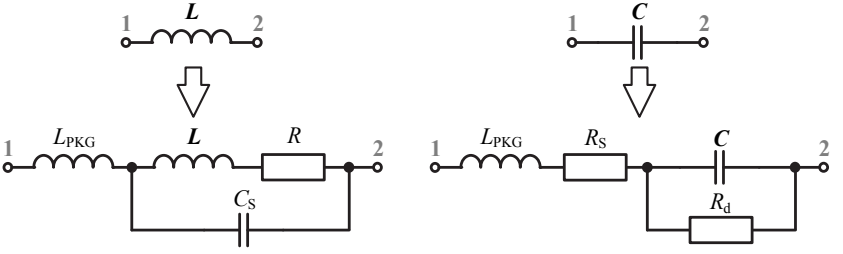


Fig. 2.2. Lumped component models: (a) inductor and (b) capacitor

Lumped inductor model, presented in Fig. 2.2a, has an equivalent impedance that can be split into resistance and reactance equations (Eroglu, 2016) presented below:

$$R_{\mathrm{L}} = \frac{R}{(1-\omega^2 LC_{\mathrm{S}}) + (\omega RC_{\mathrm{S}})^2}, \tag{2.1}$$

$$X_{\mathrm{L}} = \frac{\omega(L - R^2 C_{\mathrm{S}}) - \omega^3 L^2 C_{\mathrm{S}}}{(1-\omega^2 LC_{\mathrm{S}}) + (\omega RC_{\mathrm{S}})^2}. \tag{2.2}$$

Solving Eq. (2.2) reactance X_{L} for inductance L in gives two possible solutions:

$$L_1 = \frac{\sqrt{-4C_{\mathrm{S}}^4 R^2\omega^4 X_{\mathrm{L}}^2 - 8C_{\mathrm{S}}^3 R^2\omega^3 X_{\mathrm{L}} - 4C_{\mathrm{S}}^2 R^2\omega^2 + 1} - 2C_{\mathrm{S}}\omega X_{\mathrm{L}} - 1}{2C_{\mathrm{S}}^2\omega^3 X_{\mathrm{L}} + 2C_{\mathrm{S}}\omega^2}, \tag{2.3}$$

$$L_2 = \frac{\sqrt{-4C_{\mathrm{S}}^4 R^2\omega^4 X_{\mathrm{L}}^2 - 8C_{\mathrm{S}}^3 R^2\omega^3 X_{\mathrm{L}} - 4C_{\mathrm{S}}^2 R^2\omega^2 + 1} + 2C_{\mathrm{S}}\omega X_{\mathrm{L}} + 1}{2C_{\mathrm{S}}^2\omega^3 X_{\mathrm{L}} + 2C_{\mathrm{S}}\omega^2}. \tag{2.4}$$

Only Eq. (2.3) gives a real inductance L solution, as Eq. (2.4) provides an imaginary solution. The final value of the compensated inductor is found by subtracting the parasitic package inductance L_{pkg} from Eq. (2.3) result.

Similarly, lumped capacitor model, presented in Fig. 2.2b, has an equivalent impedance that can be split into resistance and reactance equations (Eroglu, 2016) presented below:

$$R_{\mathrm{C}} = \frac{R_{\mathrm{S}} G_{\mathrm{d}}^2 + (\omega C)^2 + G_{\mathrm{d}}}{G_{\mathrm{d}}^2 + (\omega C)^2}, \tag{2.5}$$

$$X_{\mathrm{C}} = \frac{\omega L G_{\mathrm{d}}^2 + \omega L(\omega C)^2 - \omega C}{G_{\mathrm{d}}^2 + (\omega C)^2}. \tag{2.6}$$

Solving Eq. (2.6) reactance X_{C} for capacitance C in gives two possible solutions:

$$C_1 = \frac{\sqrt{-4G_{\mathrm{d}}^2 X_{\mathrm{C}}^2 - 8G_{\mathrm{d}}^2 L_{\mathrm{pkg}}\omega X_{\mathrm{C}} - 4G_{\mathrm{d}}^2 L_{\mathrm{pkg}}^2\omega^2 + 1} - 1}{2\omega X_{\mathrm{C}} - 2L_{\mathrm{pkg}}\omega^2}, \tag{2.7}$$

$$C_2 = \frac{\sqrt{-4G_{\mathrm{d}}^2 X_{\mathrm{C}}^2 - 8G_{\mathrm{d}}^2 L_{\mathrm{pkg}}\omega X_{\mathrm{C}} - 4G_{\mathrm{d}}^2 L_{\mathrm{pkg}}^2\omega^2 + 1} + 1}{2\omega X_{\mathrm{C}} - 2L_{\mathrm{pkg}}\omega^2}, \tag{2.8}$$

Only Eq. (2.8) gives a real capacitance C solution, as Eq. (2.7) provides an imaginary solution.

Generalized inductor Q-factor has been derived as a polynomial function of frequency and inductance in the frequency range of 1 MHz – 3 GHz for different package SMD inductors and is defined by the following equations:

$$Q(f,L)=\sum_{n=0}^{2}a_n f^n, \tag{2.9}$$

$$a_n=\sum_{n=0}^{2}b_n L^n, \tag{2.10}$$

where a_n *and* b_n dimensionless coefficients, L depicts inductance in nH and f depicts frequency in Hz. Both equations are presented in a third order Taylor series form, providing the simplest yet sufficient estimate. Various component manufacturers provide similar yet differing inductor Q-factor values, whereas Eq. (2.9) and (2.10) provide a Q-factor value that is in the region of those that can be found on the market. The series could be expanded for a more accurate Q-factor curve, which more closely corresponds to that provided by any single inductor manufacturer. Table 2.1 presents the derived dimensionless coefficient values for different size SMD inductors. The following values have been derived as a result of analyzing different SMD size *Coilcraft* (Coilcraft Inc. RF Inductor Finder, 2019) inductors.

Table 2.1. Inductor Q-factor estimation for different surface mount component packages

Package	Coefficient	b_2	b_1	b_0
0201 size inductor	$a_0 \rightarrow$	-9.7×10^{-2}	1.04	4.5
	$a_1 \rightarrow$	-2.5×10^{-10}	2.9×10^{-9}	2.7×10^{-8}
	$a_2 \rightarrow$	5.7×10^{-20}	-4×10^{-19}	-4×10^{-18}
0402 size inductor	$a_0 \rightarrow$	-4.2×10^{-2}	1.08	6.04
	$a_1 \rightarrow$	-6.86×10^{-11}	2.57×10^{-9}	4.47×10^{-8}
	$a_2 \rightarrow$	1.04×10^{-20}	5.2×10^{-20}	-5.24×10^{-18}
0603 size inductor	$a_0 \rightarrow$	2.46×10^{-2}	-8.52×10^{-1}	12.8
	$a_1 \rightarrow$	7.27×10^{-11}	-2.31×10^{-9}	5.08×10^{-8}
	$a_2 \rightarrow$	1.14×10^{-20}	-5.83×10^{-19}	2.44×10^{-18}
0805 size inductor	$a_0 \rightarrow$	2.08×10^{-3}	1.17×10^{-1}	11.76
	$a_1 \rightarrow$	-3.37×10^{-12}	-2.69×10^{-10}	7.78×10^{-8}
	$a_2 \rightarrow$	1.7×10^{-20}	-1.48×10^{-18}	-5.92×10^{-18}
1206 size inductor	$a_0 \rightarrow$	-4.63×10^{-3}	8.35×10^{-1}	10.4
	$a_1 \rightarrow$	1.13×10^{-12}	-6.23×10^{-10}	8.16×10^{-8}
	$a_2 \rightarrow$	2.48×10^{-21}	-2.5×10^{-19}	-1.7×10^{-17}

SMD inductor *SRF* has been approximated as a function of inductance value by the following equation

$$SRF \approx 20/\sqrt{L}, \tag{2.11}$$

where L is inductance in nH and *SRF* is in GHz. The latter equation has been derived by analyzing *0402HP* series *Coilcraft* inductors (Coilcraft Inc. RF Inductor Finder, 2019) with values from 1 nH to 150 nH and curve-fitting the data to create a generalized equation. Inductor *ESR* is found from the following

equation (Bowick, 2007), which describes the relationship between *Q*-factor and reactance

$$Q_L = X_L / ESR_L . \tag{2.12}$$

Generalized capacitor *ESR*, has been derived as a polynomial function of frequency and capacitance for different package SMD capacitors and is defined by the following equations

$$ESR(f, C) = \sum_{n=0}^{2} m_n f^n , \tag{2.13}$$

$$m_n = \sum_{n=0}^{2} k_n C^n , \tag{2.14}$$

where m_n and k_n are dimensionless coefficients, C depicts capacitance in pF and f depicts frequency in Hz. Similarly to Eq. (2.9) and Eq (2.10), Eq. (2.13) and Eq (2.14) are presented in a third order Taylor series form, providing the simplest yet sufficient estimate. Various component manufacturers provide similar yet differing capacitor *ESR* values, whereas Eq. (2.13) and Eq (2.14) provide an *ESR* value that is in the region of those that can be found on the market. The series could also be expanded for a more accurate *Q*-factor curve, which closely corresponds to that provided by a single inductor manufacturer. Capacitor *ESR* estimation coefficients, presented in Table 2.2, have been derived by analyzing capacitors from two major capacitor manufacturers *Murata* (Murata Chip Multilayer Ceramic Capacitors for General Purpose GRM series, 2019) and *TDK* (TDK Multilayer Ceramic Chip Capacitors, 2019).

Table 2.2. Capacitor equivalent series resistance estimation for different surface mount component packages

Package	Coefficient	k_2	k_1	k_0
0201 size capacitor	$m_0 \rightarrow$	4.71×10^{-3}	-1.31×10^{-1}	9.09×10^{-1}
	$m_1 \rightarrow$	-6.01×10^{-14}	1.49×10^{-12}	-3.44×10^{-12}
	$m_2 \rightarrow$	-7.22×10^{-24}	3.83×10^{-22}	8.4×10^{-22}
0402 size capacitor	$m_0 \rightarrow$	4.84×10^{-3}	-1.35×10^{-1}	8.93×10^{-1}
	$m_1 \rightarrow$	-7.94×10^{-14}	2.99×10^{-12}	-5.07×10^{-12}
	$m_2 \rightarrow$	-2.66×10^{-23}	7.31×10^{-22}	1.93×10^{-21}
0603 size capacitor	$m_0 \rightarrow$	2.6×10^{-4}	-1.51×10^{-2}	3.86×10^{-1}
	$m_1 \rightarrow$	2.05×10^{-13}	-1.26×10^{-11}	1.75×10^{-10}
	$m_2 \rightarrow$	-3.95×10^{-23}	2.44×10^{-21}	-2.3×10^{-20}

The analyzed capacitors had values of 0.1 pF, 0.5 pF, 1 pF, 5 pF, 10 pF, 18 pF, 20 pF and 40 pF across 0201, 0402, 0603, 0805 and 1206 packages.

Larger size (0805 and 1206) capacitors have an almost identical *ESR* curve to that of 0603 capacitors. As a result coefficients for 0603 size capacitor can be

used approximating *ESR* for both 0805 and 1206 size capacitors, hence are not included in Table 2.2.

Capacitor parasitic dielectric drain (leakage) resistance $R_d = 1/G_d$ is dependent on the type of dielectric material used. The most widely used dielectric materials and their *ESR* and parasitic drain resistance R_d have been summarized analyzing (Kemet Surface Mount Multilayer Ceramic Chip Capacitors commercial grade X5R dielectric, 2018a; Kemet Surface Mount Multilayer Ceramic Chip Capacitors commercial grade X7R dielectric, 2018b; Cain, 2019 & CDR Multilayer Ceramic Capacitors – Performance Characteristics, 2019) and are presented in Table 2.3.

Table 2.3. Surface mount component capacitor parasitic drain resistance

Dielectric type	R_d, GΩ
NPO	100
X7R	
X5R	50

SMD inductor and capacitor packages have typical *ESL* and *ESR* values that are presented in Table 2.4. The following parameters have been summarized by analyzing technical datasheets (Renesas Choosing and Using Bypass Capacitors, 2011; Kemet Surface Mount Multilayer Ceramic Chip Capacitors commercial grade X5R dielectric, 2018a; Kemet Surface Mount Multilayer Ceramic Chip Capacitors commercial grade X7R dielectric, 2018b; Cain, 2019 & CDR Multilayer Ceramic Capacitors – Performance Characteristics, 2019).

Table 2.4. Surface mount component packages and their typical equivalent series resistance and inductance

Package	*ESL*, pH	*ESR*, mΩ
0201	400	40
0402	550	49
0603	700	77
0805	800	67
1206	1250	99

The final compensated inductor or capacitor value is found by inserting reactance X_L or X_C, calculated using classical impedance matching theory, into Eq. (2.3) or Eq. (2.7) accordingly, taking into account the derived component parasitics estimation equations Eq. (2.9) – Eq. (2.10) and Eq. (2.13) – Eq. (2.14), typical SMD package parasitics (Table 2.3 and Table 2.4) and following the proposed algorithm in Fig. 2.1.

It is to be noted, that the derived equations provide generalized models that are suited not only to provide exact *Coilcraft*, *Murata* or *TDK* component values. The latter equations do not exactly match the *Coilcraft*, *Murata* or *TDK* part

parameter curves, but provide a parameter change tendency, which is true to SMD capacitors and inductors in general, regardless of the manufacturer.

The proposed mathematical model and *IMNS* algorithm evaluation through simulation and measurement are presented in the following sections.

2.2. *IMNS Toolbox* Plug-in for *Cadence Virtuoso*

The proposed methodology of estimating the main parasitic component parameters and *IMNS* algorithm have been implemented as an *IMNS Toolbox* plug-in into the professional IC design software *Cadence Virtuoso*. The graphical user interface (GUI) has been created using *SKILL* programming language, whereas the mathematical processing has been implemented in *OCEAN* programming language. The latter software can work as either a plug-in, accessible through the *Virtuoso* window, shown in Fig. 2.3, or as a script (without GUI). The full program contains more than 6000 lines of *OCEAN/SKILL* code and can run on both older (version 5) and newer (version 6) *Cadence Virtuoso* software builds.

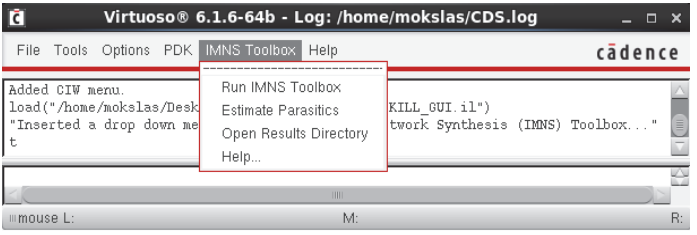


Fig. 2.3. *IMNS* toolbox drop-down menu in *Cadence Virtuoso* window

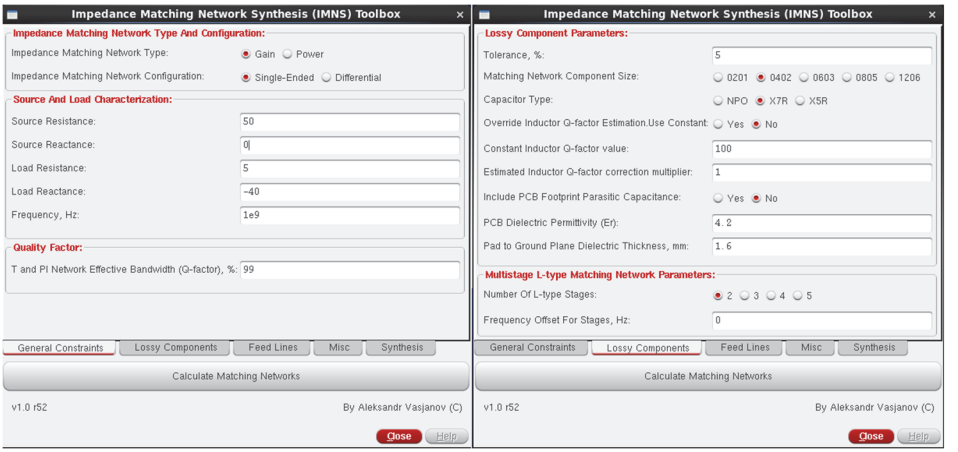
The following functions have been implemented in the proposed *IMNS Toolbox*:

1. Fully complex load and source matching capability;
2. Single-stage/multi-stage *L*-type, *π*-type, *T*-type in both single-ended and differential configurations;
3. Solutions with both lossless (ideal) and lossy (compensated) components calculation;
4. Different component package parasitics options (component size, tolerance, dielectric type, *Q*-factor estimation, PCB footprint pad capacitance inclusion);
5. Different length feed line between source and load impact inclusion;
6. A tool for estimating lossy component parasitics and plotting them in a graphical window. *Q*-factor can be plotted for different inductor SMD packages and inductance values, as well as *ESR* for different SMD packages and capacitance values. The latter tool can be used to compare

the estimated parameters to those presented in the datasheet of the selected component.

7. Designed matching network synthesis and automatic simulation. All ideal and lossy (including all estimated component package parasitics) matching networks are synthesized in a chosen *Cadence Virtuoso* library. Each synthesized matching network undergoes automatic small-signal *S*-parameter simulation saving all graphical results as pictures and extracting data into the final report file.
8. Report generation with an option of sending it to a provided *e*-mail address. The report file contains constraints, matching network topologies with their corresponding ideal and lossy (compensated) solutions, simulation results as and simulation run time.

The *IMNS Toolbox* "General Constraints" and "Lossy Components" tabs are presented in Fig. 2.4.



(a) (b)

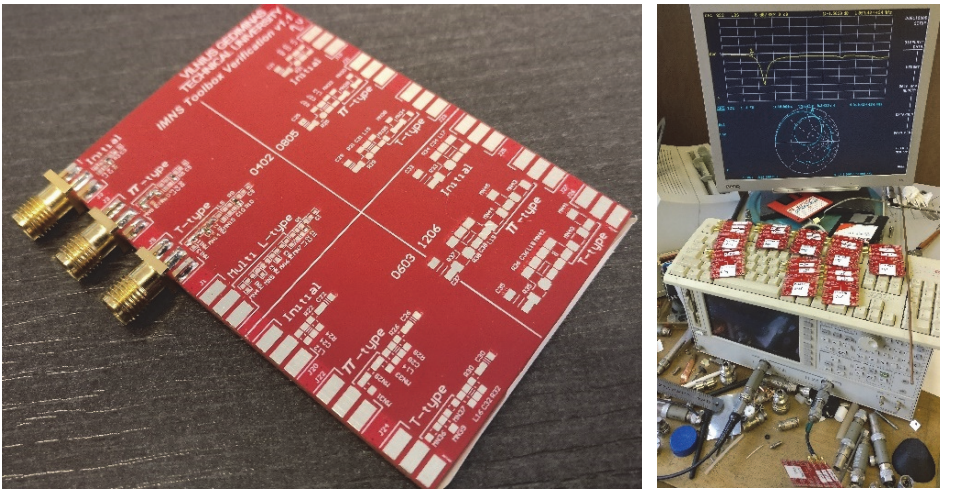
Fig. 2.4. *IMNS Toolbox*: (a) General Constraints and (b) Lossy Components tabs

The tabs presented in Fig. 2.4 are used to define the main impedance matching constraints and provide information on the type and size of surface mount components. All of the latter information is taken into account when calculating the impedance matching network component values using classical theory and applying the proposed compensation methodology.

The proposed *IMNS Toolbox* plugin reduces the number of simulation and measurement iterations required to match a given source impedance to a load impedance at a certain frequency. Usually one iteration is required when matching in the range from 1 MHz to 1 GHz and one to three iterations when matching in 1 GHz to 3 GHz.

2.3. Measurement Test Setup

Two PCBs have been designed in order to evaluate the compensation, which is provided by the proposed mathematical model and *IMNS* algorithm. Fig. 2.5 presents a designed test PCB to conduct experimental research on matching source and complex load (Fig. 2.5a). The designed PCB has single-stage and multi-stage *L*-type, as well as π-type and *T*-type matching network PCB footprints for different component package size (0201, 0402, 0603, 0805 and 1206). Moreover, both PCBs have been fabricated with a controlled impedance option in order to maintain a constant $Z_0 = 50\ \Omega$ microstrip impedance. The target research range is mid-band 5G frequencies, which include both licensed (up to 6 GHz) and unlicensed (5.9–7.1 GHz) bands.



(a) (b)

Fig. 2.5. (a) Impedance matching network algorithm test printed circuit board and (b) measurement setup using *HP8753E* vector network analyzer

Measurements have been conducted using a calibrated *HP8753E* (Fig. 2.5b) vector network analyzer (VNA). All measurement equipment has been calibrated using "Open/Short/Load" technique.

2.4. Simulation and Measurement Results

The proposed mathematical model and *IMNS* algorithm have both been evaluated via computer simulation and experimental measurement. Computer simulation has been conducted using the created *IMNS* toolbox for *Cadence*

Virtuoso, presented in Chapter 2.2, whereas experimental measurements have been done using the test-bench described in Chapter 2.3.

Computer simulation evaluated *L*-type, π-type and *T*-type matching networks, designed to match a source impedance of Z_S=50 Ω to measured load impedances of $Z_{L,0.5GHz} = 10.4 + j11.1$, $Z_{L,1.5GHz} = 14.6 + j36.6$ and $Z_{L,3GHz} = 54.3 + j111$ using 0402 (the most widely used part sizes in the consumer electronics industry) size SMD components at frequencies of 0.5 GHz, 1.5 GHz and 3 GHz. The same networks in both ideal and compensated component solutions have been evaluated through measurement – firstly, component values calculated using classical theory have been used in the measurement test-bench and components with compensated values afterwards.

Results presented in Fig. 2.6, Fig. 2.7 and Fig. 2.8 plot three curves associated with each target frequency. "*Sim. Non-compensated*" curves (dotted) correspond to the simulation of matching networks with non-compensated component values, which are found using classical impedance matching theory, with all package parasitics included. "*Meas. Non-compensated*" curves (dashed) correspond to measurement results, when non-compensated component value are used (found using classical impedance matching theory). Finally, "*Meas. Compensated*" curves (solid) correspond to measurement results, when compensated component values, which have been calculated using the proposed mathematical model and *IMNS* algorithm, are used.

Fig. 2.6 presents 0402 size *L*-type matching network simulation and measurement results accordingly at the frequency of 0.5 GHz. 10% tolerance SMD inductors and capacitors are used during experimental measurements. Analysis of the presented measurement results show that the impedance matching network with compensated values matches the source and load at a frequency of 0.504 GHz, when the target was 0.5 GHz.

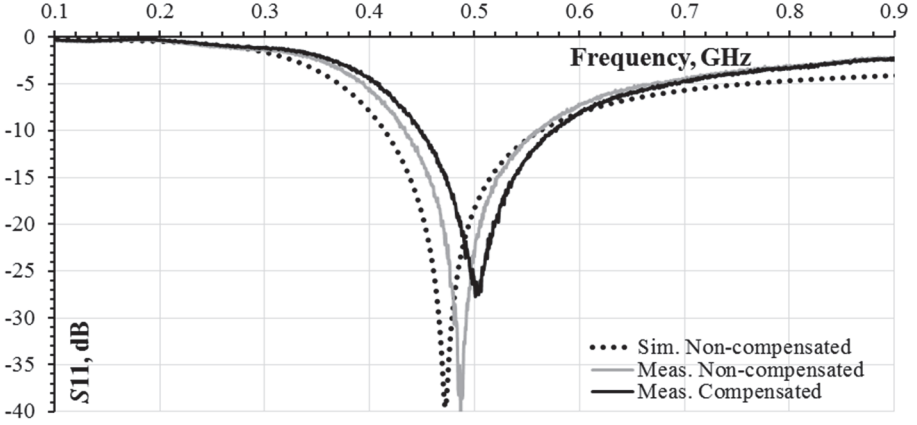


Fig. 2.6. 0402 size *L*-type matching network research results at 0.5 GHz

This proposed methodology minimizes the offset to 0.08% deviation (compared to 1% offset achieved with component values calculated using classical theory). Further analysis involves multiple impedance matching networks and the results reveal that at a target frequency of 0.5 GHz components with a 10% tolerance, parasitics and non-compensated values provide 3.2–9.8% target frequency deviation. When using the same tolerance components at 0.5 GHz, matching networks with compensated values, the unwanted offset range becomes 0.1–8.8% from the target frequency. The proposed compensation algorithm reduced the worst-case deviation by 1% at 0.5 GHz.

Fig. 2.7 presents 0402 size *T*-type matching network simulation and measurement results accordingly at the frequency of 1.5 GHz, which is included in the mid-band 5G frequency range. 10% tolerance SMD inductors and capacitors were used during experimental measurements.

The latter figure reveals smaller S_{11} value at the notch frequency, which is generally affected by the component tolerance and the closest available component values to the calculated ones.

Nevertheless, the proposed compensation algorithms matched the circuit at 1.47 GHz compared to the 1.44 GHz using the non-compensated values. This leads to a deviation improvement of 2.16%, from 4.16% to 2% deviation. Further insight into multiple matching networks at 1.5 GHz revealed, that a 4–12.3% undesired offset from the target frequency can be introduced using 10% tolerance components using non-compensated values. Applying the proposed correction, the deviation region is reduced to 1–8.7% from the target frequency which is a 3.6% improvement at the worst case offset.

Fig. 2.8 presents 0402 size *T*-type matching network simulation and measurement results accordingly at the frequency of 3 GHz, also included in the mid-band 5G wireless frequency range.

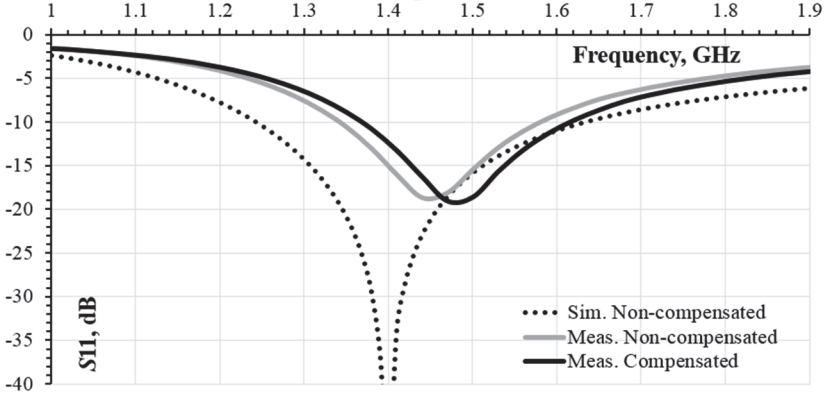


Fig. 2.7. 0402 size *T*-type matching network research results at 1.5 GHz

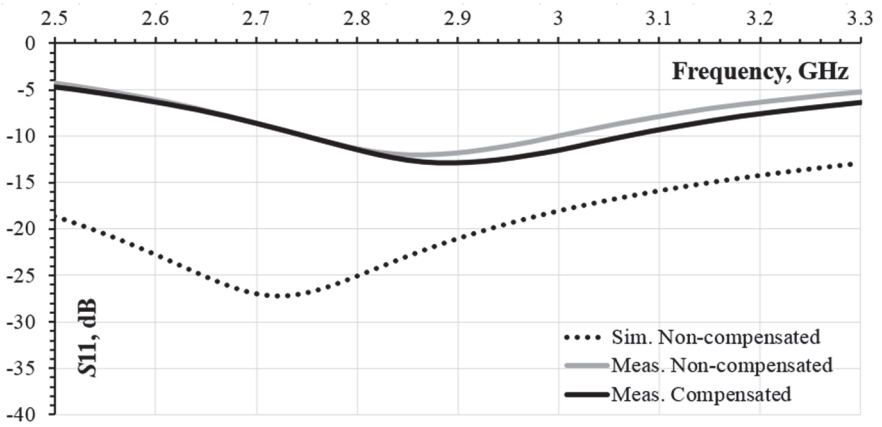


Fig. 2.8. 0402 size *T*-type matching network research results at 3 GHz

10% tolerance SMD inductors and capacitors were used during experimental measurements. The presented frequency responses conclude, that 10% tolerance components are not sufficient enough to provide exact (or within several percents) impedance matching at 3 GHz. The compensated values improve the response and shift the curve from 2.845 GHz to around 2.9 GHz, but the target frequency is not reached. As a result, the deviation range of using compensated matching network component values reduces from 5.5–15.1% to 1.3–8.1% at a target frequency of 3 GHz.

L-type and *T*-type matching network topologies have been presented in Chapter 1.2.2 of this dissertation in Fig. 1.27 and Fig. 1.28. The results presented in Fig. 2.6, Fig. 2.7 and Fig. 2.8 have been obtained using components in listed Table 2.5.

Table 2.5. 0402 size impedance matching network component values

0402 matching network type		Matching network component values		
		0.5 GHz	1.5 GHz	3 GHz
L, *T*	Non-compensated	Forward *L*-type L_1 = 7.86 (8.2) nH C_2 = 11.43 (11) pF	*T*-type C_1 = 17.7 (18) pF L_2 = 3.18 (3.3) nH C_3 = 1.78 (1.8) pF	*T*-type C_1 = 3.58 (3.6) pF L_2 = 8.58 (8.2) nH C_3 = 0.47 (0.5) pF
	Compensated	Forward *L*-type L_1 = 7.47 (7.5) nH C_2 = 10.87 (11) pF	*T*-type C_1 = 10.67 (11) pF L_2 = 2.78 (2.7) nH C_3 = 1.69 (1.6) pF	*T*-type C_1 = 2.3 (2.2) pF L_2 = 6.83 (6.8) nH C_3 = 0.45 (0.5) pF

The number presented outside the brackets depicts the calculated value, while the value given inside the brackets is the closest manufactured component value to the calculated one. *GRM155R71H* series 0402 SMD capacitors and *LQG15HS* series 0402 SMD inductors both manufactured by *Murata* have been used during

measurements. Components with the index "1" at the source side, whereas components with index "2" in the case of the *L*-type network and index "3" in the case of the *T*-type network – on the load side.

Due to the unknown exact value (including the deviation introduced by the component tolerance) of each component used, it is not clear what tolerance components are sufficient to provide accurate matching (within 1–2% of the target frequency).

In order to find out whether or not 10% components can be used as matching network building blocks at high frequencies (2 GHz and above), a series of simulations have been conducted with the results presented in Fig. 2.10 and Table 2.6.

Table 2.6. Yield results at 2.5 GHz target frequency

Yield, %	Number of passed/failed circuits	Target specification/comment
81.9	819/181	All components 10%, $S_{11} \leq -10$ dB in the range on 2.4–2.6 GHz
99.3	993/7	All components 5%, $S_{11} \leq -10$ dB in the range on 2.4–2.6 GHz
98.7	987/13	C_2 tolerance 5%, C_1 and L_1 tolerance 20%, $S_{11} \leq -10$ dB in the range on 2.4–2.6 GHz

An insight on a *T*-type matching network with 10% tolerance components at 2.5 GHz target frequency is presented in Fig. 2.9. When all compensated component values ($C = 14.38$ pF, $L = 3.15$ nH, $C = 0.59$ pF) are reduced by 10%, the simulated response is as shown in the dotted line in Fig. 2.9 alongside with the measured results. The fact that simulation results in Fig. 2.9 are similar to the measurement results, implies that the lumped component models and the proposed parasitic parameter prediction algorithm performs with high accuracy and is viable when designing impedance matching networks. The measurement results in presented Fig. 2.9 do not suffice the requirement to match the circuit at 2.5 GHz due to low component tolerance. The latter leads to a statement, that in order to achieve high impedance matching network response accuracy (of around 1% at the target frequency), low tolerance components (5%, 2% or even 1%) should be used alongside the proposed compensation algorithm that at high frequencies (above 2 GHz). At frequencies below 2 GHz, 10% tolerance components provide sufficient S_{11} curve accuracy.

The next logical step arising from the previous paragraph is to understand what component tolerance is sufficient at frequencies above 2 GHz. Component price is tightly related to its tolerance while reducing the cost of the bill of materials is paramount for high volume production. A statistical yield analysis has been conducted on a *T*-type matching network at a target frequency of 2.5 GHz (an already existing 5G LTE band B41) with the results shown in Fig. 2.10.

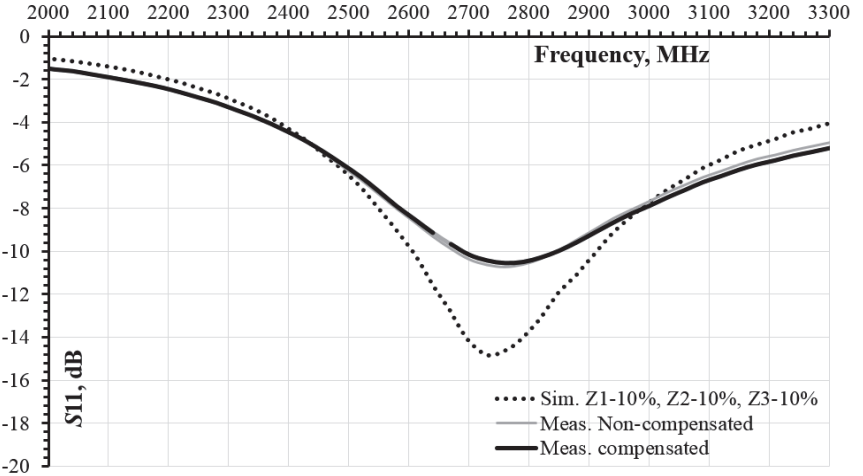


Fig. 2.9. 0402 size *T*-type matching network research results at 2.5 GHz

Each of the three graphs depicts the yield when one of the three component values has changed in the range related to the tolerance of the component. The selected number of samples was chosen to be 1000 and the target yield specification was chosen to be $S_{11} \leq -10$ dB in the frequency range from 2.4 GHz to 2.6 GHz. The estimated parasitic parameters for each component in the matching network are kept constant, whereas the value (capacitance or inductance) is changed based on the selected tolerance and value in the range of three standard deviations (3σ). Based on the results presented in Fig. 2.10, component C_3 (closest to the load) was the most susceptible to tolerance shifts and mostly defined the yield. In other words, the latter component introduced the most frequency shift to the S_{11} response. All three graphs in Fig. 2.10 present components with 5% and 10% tolerances and one can clearly spot that at frequencies above 2 GHz (in this case at a frequency of 2.5 GHz) 10% tolerance components do not provide sufficient yield (above 95%) with the given target requirements.

The newly proposed IMNS algorithm and mathematical models reduce the number of simulation and measurement cycles, when designing *L*-, *π*- and *T*-type matching networks: up to 1 simulation and measurement cycle in the range from 1 MHz to 1 GHz and 1 to 3 cycles when the frequency range is 1–3 GHz.

Results presented in Table 2.6 are related to the histograms in Fig. 2.10 and depict that 5% components provide a 99.3% yield at 2.5 GHz. It has been mentioned that based on the results in Fig. 2.10, component C_2 value greatly affects the yield, and therefore the last row of the table displays a situation, when C_2 tolerance is kept low (5%), but the tolerance of C_1 and L_1 is increased to that of standard general purpose components (20%). This resulted in a decrease in the

yield only by 0.6%. This leads to a conclusion that in order to have a ≥95% yield of matched circuits at a target frequency above 2 GHz, 5% component tolerance is sufficient. An additional step can be taken to reduce the price of a mass-produced consumer product without sacrificing the yield.

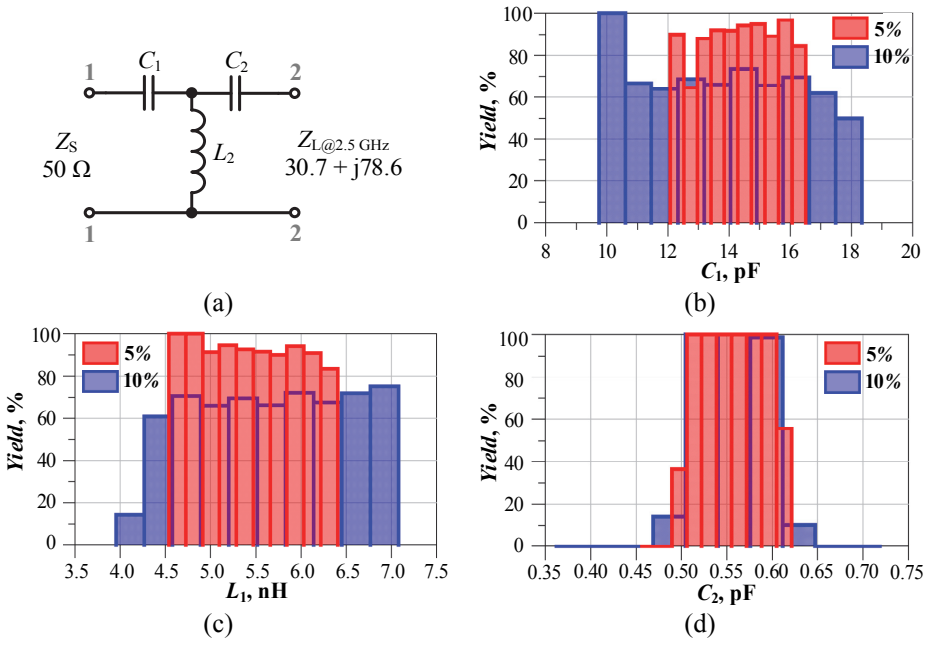


Fig. 2.10. Yield analysis of a matching network at 2.5 GHz with different tolerance components: (a) Test circuit and load conditions; (b) component C_1 value changed within tolerance with L_1 and C_2 values kept constant; (c) component L_1 value changed within tolerance with C_1 and C_2 values kept constant; (d) component C_2 value changed within tolerance with C_1 and L_1 values kept constant

One can find the component in the matching network, which is most responsible to the shift of the S_{11} curve in the frequency axis and replace this component with a 5% tolerant part while simultaneously reducing the tolerance of the rest of the matching network components to the cheapest 20% tolerance versions.

Fig. 2.11 presents Monte Carlo simulation results for the matching network in 2.4–2.6 GHz frequency range. The latter figure presents histograms with minimal S_{11} response values (at the notch frequency) on the horizontal axis and the number of circuits that satisfy the latter condition on the vertical axis. Three types of component tolerances are used during Monte Carlo simulation and correspond to each histogram in Fig. 2.11. The total area for each of the latter

three histograms is identical. The histograms depict the number of circuits with different S_{11} response minimal value offsets from the target 2.5 GHz frequency due to component tolerance. According to the pink histogram, that depicts the circuit performance with 10% tolerance components, in many cases (181 out of 1000) the response is shifted in a way that S_{11} value shifts above the −10 dB

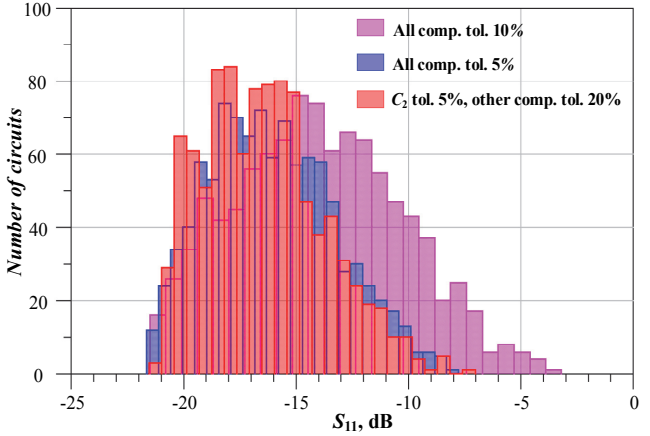


Fig. 2.11. Monte Carlo simulation results in the frequency range of 2.4–2.6 GHz, when different tolerance matching network components are used

threshold. This leads to a total yield of 81.9%, as presented in Table 2.6. In the case of 5% components, the number of failed circuits is less, resulting in negligible S_{11} curve shifts around the target frequency.

As previously mentioned, in order to reduce the number of high tolerance components (and subsequently the overall price) without greatly affecting the S_{11} response and yield, the component that is most susceptible to value shifts (C_2 in the case of Fig. 2.10) is kept at 5% tolerance, whereas all other components are kept at a general purpose 20% tolerance level. According to the Monte Carlo simulation results that are shown in Fig. 2.11, the red histogram spread is similar to the blue histogram in the frequency range of interest. This directly implies that the S_{11} curve frequency deviation is similar for matching networks with all 5% tolerance components to those with C_2 at 5% and all other component tolerances kept at a general purpose 20%. Only a negligible number of occurrences when $S_{11} > -10$ dB in in both cases, resulting in a similar yield as provided in Table 2.6. The simulation results in Fig. 6 confirm the proposition that in order to reduce the BOM cost during mass production, only the most sensitive to change component in the impedance matching network needs to be high precision and all other component tolerances can be kept in the standard general-purpose range.

The results, presented in Fig. 2.6, Fig. 2.7, Fig. 2.8, Fig. 2.9, Table 2.5 and Table 2.6, can be summarized that the proposed algorithm improves the precision of calculating compensated SMD component based impedance matching networks by 1–6% relative to the target frequency. The proposed component value algorithm is viable to be used during impedance matching network design up to 3 GHz. Impedance matching network precision is dependent on the tolerance of used components in the whole frequency range, but according to measurement results components with 10% tolerance are not recommended at frequencies higher than 2 GHz. Based on the results, presented in Fig. 2.10 and Fig. 2.11, 5% components responsible for shifting the S_{11} parameter plot will suffice in the frequency range of 2–3 GHz. Moreover, it is possible to define components in the matching network and keep their tolerance at 5%, while keeping other component at lower tolerance according to the IEC/EN 60062 standard without affecting the yield.

The proposed IMNS algorithm is suitable for both low- and mid-band 5G frequency ranges and the impact of compensating parasitic parameters at a target frequency of 6.5 GHz in the unlicensed 5G band is presented in Fig. 2.12.

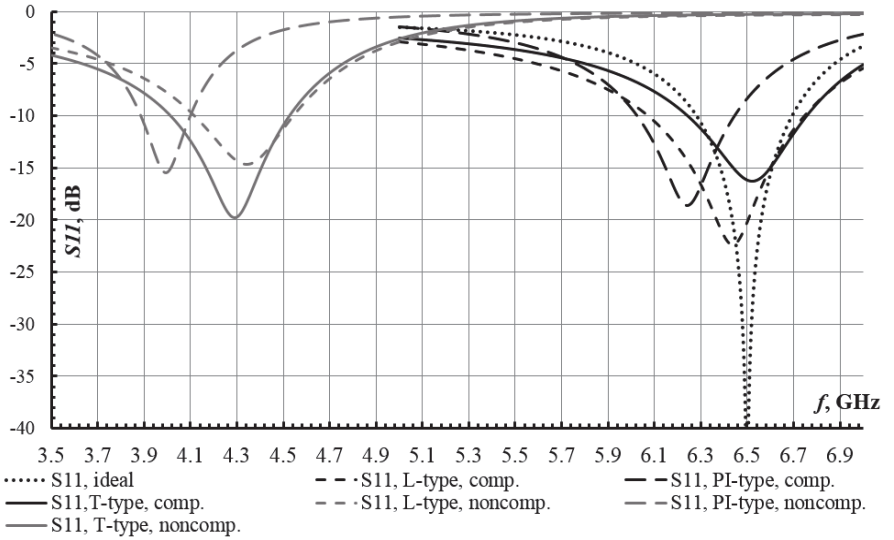


Fig. 2.12. Proposed algorithm simulations at mid-band 5G frequency range

Three lumped impedance matching network configurations (single-ended *L*-, *π*- and *T*- type) are investigated. The source impedance is set to be $Z_S = 50\ \Omega$, whereas the load impedance is set to be $Z_L = 7 + j35$. The black curves coorespond to the S_{11} responses for matching networks with compensated values, whereas the grey curves define the S_{11} response for matching networks without the proposed

compensation. Parasitic parameters are estimated and included in both cases. Concluding the results, presended in Fig. 2.12, the proposed IMNS algorithm reduces the maximum offset from the target frequency up to 300 MHz (4.6% from the target frequency), compared to 1.5 GHz (23% from the target frequency) offset without the proposed compensation.

2.5. Second Chapter Conclusions

Research results presented in Chapter 2 address dissertation problem No. 2, raised in Chapter 1 conclusions section. Chapter 2 can be summarized with the following concluding statements:

1. Lumped impedance matching network components (capacitors and inductors) have parasitic parameters, which affect the overall frequency response. Classical matching network design theory does not take them into account. As a result, a methodology of estimating the main parasitic component parameters as functions of surface mount device package size, frequency and main parameter (capacitance or inductance) value alongside with a compensation algorithm has been proposed. An impedance matching network synthesis (*IMNS*) algorithm has been proposed based on the research results. The latter algorithm has been implemented as an *IMNS Toolbox* plug-in and included in the professional IC design software *Cadence Virtuoso*.
2. A novel methodology of estimating the main parasitic parameters for lumped inductors and capacitors has been introduced within the proposed *IMNS* algorithm. The following impact on impedance matching accuracy has been measured when the estimated parasitic parameters are taken into account: a 0.08% (0.92% improvement compared to the deviation when using classical theory which doesn't include lumped component parasitic parameters) deviation when the target frequency is 0.5 GHz, a 2% deviation when the target frequency is 1.5 GHz (2.16% improvement over classical theory) and 3.3% (3.3% improvement over classical theory) deviation when the target frequency is 3 GHz. 0402 size surface mount components were used to obtain experimental results. Simulations in the 6.5 GHz range revelaed a maximum offset from the target frequency reduction by 18.4%.
3. Impedance matching network component value (capacitance and inductance) tolerance is an important parameter, which affects the

accuracy of the S_{11} curve frequency response. Theoretical and experimental analysis of multiple impedance matching network results and revealed that at a target frequency of 0.5 GHz components with a 10% tolerance, parasitics and non-compensated values provide 3.2–9.8% target frequency deviation. The proposed compensation algorithm reduced the worst-case deviation by 1% at 0.5 GHz. The same components provided 4–12.3% (non-compensated) and 1–8.7% (compensated) target frequency deviation ranges at 1.5 GHz. The deviation range of using compensated matching network component values increases from 5.5–15.1% to 1.3–8.1% at a target frequency of 3 GHz. As a result, the proposed algorithm reduces the worst-case frequency response offset by 1–7% compared to that of the classical theory.

4. Experimental research results revealed, that 10 % tolerance components can shift the S_{11} response by 1–5% at frequencies of up to 2 GHz which can be held as sufficient, but more accurate value components are required at frequencies over 2 GHz to obtain sufficient results. According to the results obtained during simulation and experimental research, worst-case frequency offset at 2.5 GHz using 5% tolerance components is only 80 MHz. The improvements to the matching response accuracy using higher precision components (2% or 1%) compared to their unit price make their usage untenable compared to 5% tolerance components. On the other hand, lower tolerance components according to the IEC/EN 60062 standard should be chosen if the budget is not of great importance and accuracy is the main priority.

3

Radio Frequency Power Amplifier Research, Design and Synthesis

The first part following chapter presents research results for different arrangements of classical RF PAs and TWAs. The simulation and measurement results, designed and fabricated ASIC pictures as well as conclusions are also included. The second part of the following chapter contains a comparison of two DPAs, which are suitable for low power mid-band 5G wireless devices. The step-by-step guide of designing a DPA with both a classical and simplified impedance inverters are presented followed by a performance comparison and conclusions. Research results presented in this chapter address dissertation problem No. 1, raised in Chapter 1 conclusions section – researching and defining the most promising RF PA architecture suitable for low- to mid-power portable mid-band 5G applications which provides IF bandwidths of more than 150 MHz as well as improved efficiency, compared to the classical PAs,

The research results presented in this chapter have been included in a *Clarivate Analytics Web of Science* databases referred publication (Vasjanov & Barzdenas 2017) with a citation index.

3.1. Different Power Amplifier Architectures and Their Synthesis Algorithms

This subsection presents simulation and measurement results for the designed and fabricated ASICs – one with classical PA configurations and another with TWA solutions. The variations in classical PA architectures are used to define the performance differences and act as a benchmark for achievable specifications 0.13–0.18 μm CMOS processes. The TWA research is also included, as it is one of the promising advanced architectures and receives non-stop attention in the published articles for the last decade.

According to the advanced PA architecture analytical research results, presented in Chapter 1 of this dissertation, two of the published four architectures are selected for further comprehensive theoretical and experimental investigation. The latter advanced architectures are DPA and TWA. ET/EER and outphasing PAs are not suited to be implemented in 5G devices due to their complexity, intermediate frequency bandwidth and linearization limitations, as well as additional noise injected in the transmitted signal. Different configurations of classical PAs are also a part of this study, as the classical PA is the basis of both DPA and TWA.

3.1.1. Classical Radio Frequency Power Amplifier Architecture Variations

The first designed ASIC contains four independent classical configuration PAs with the simplified schematics presented in Fig. 3.1 and the layout alongside the fabricated IC given in Fig. 3.2. All PAs shown in Fig. 3.1 utilize a cascode configuration, which is shown as a double gate *n*-channel metal-oxide semiconductor (NMOS) field effect transistor. The supply voltage for all PAs is 1.6 V. V_{cascode} is used as gain control as the power transistor is split into four parallel devices. Package parasitics and *ESD* diodes (D1 and D2) are also included.

The first PA simplified schematic is shown in Fig. 3.1 by the name of PA1 and located in the bottom right quadrant of the fabricated IC in Fig. 3.2. PA1 is a single transistor classical amplifier configuration with all matching components as well as biasing left off-chip.

The second and third PAs, PA2 and PA3 on Fig. 3.1 accordingly, are cascode solutions with and without an *RC* feedback circuit. The latter amplifiers include input DC block capacitor and impedance matching response tuning as well as biasing circuits and are presented in the left top and bottom quadrants of the fabricated IC in Fig. 3.2. The *RC* feedback circuit improves the stability of the PA and can be used to widen the matching bandwidth.

The fourth PA is identical to the cascode one without an *RC* feedback circuit but contains an input bias block, which also acts as an input stage. The input stage is a buffer with a feedback resistor with the transistors sized to form a *VDD*/2 bias voltage at the gate of the output stage. PA4 is placed in the right and bottom quadrants of the fabricated IC in Fig. 3.2.

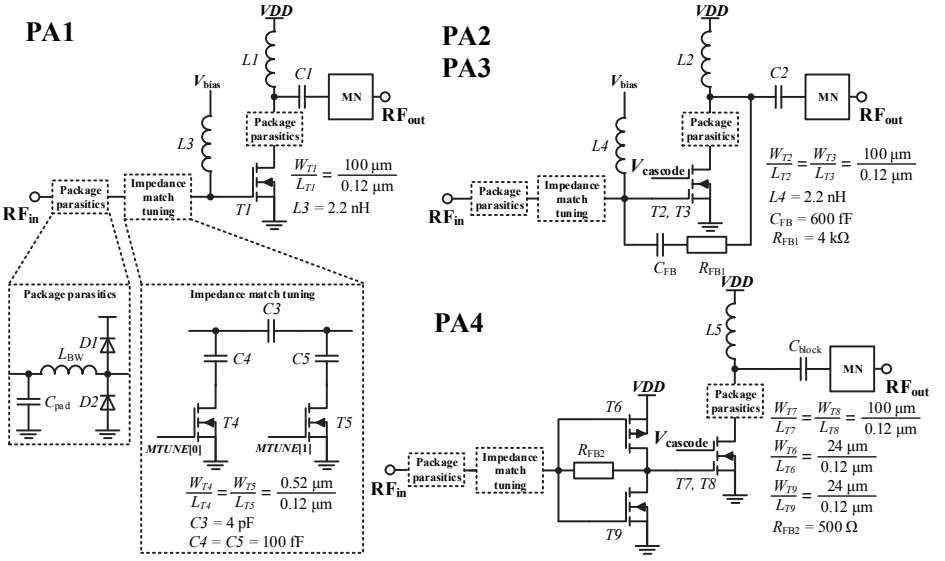
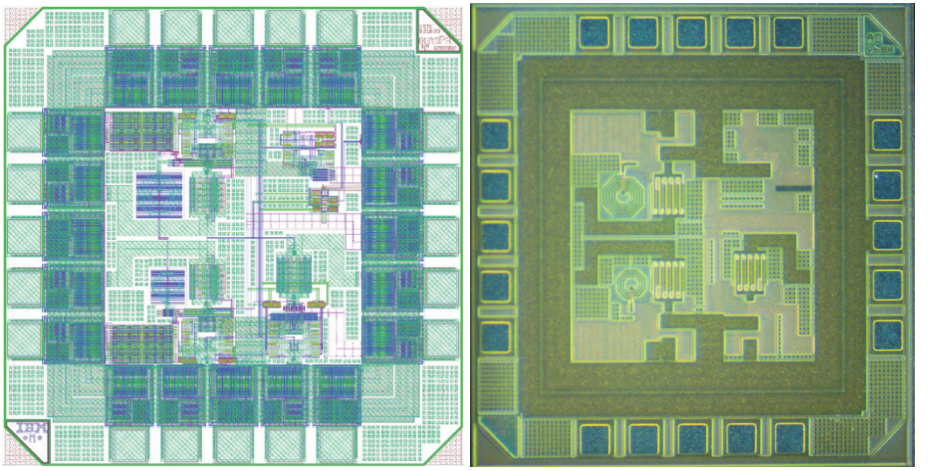


Fig. 3.1. *IBM* 0.13 µm CMOS quad power amplifier chip simplified schematic

The output impedance matching circuit as well as the RF choke are off-chip and are placed externally on the test-bench PCB.



(a) (b)

Fig. 3.2. *IBM* 0.13 µm CMOS quad power amplifier chip: (a) layout; (b) fabricated IC.

The designed classical PAs are simulated under three operating condition sets: typical *TT* corner (40 °C operating conditions, typical NMOS and PMOS transistor parameter models), slow *SS* corner (80 °C operating conditions, worst-case fabricated NMOS and PMOS transistor parameter models) and fast *FF* corner (−40 °C operating conditions, best-case fabricated NMOS and PMOS transistor parameter models). Only typical corner simulation results are presented below.

Small-signal *S*-parameter simulation and measurement results for all designed PAs are presented in Fig. 3.3.

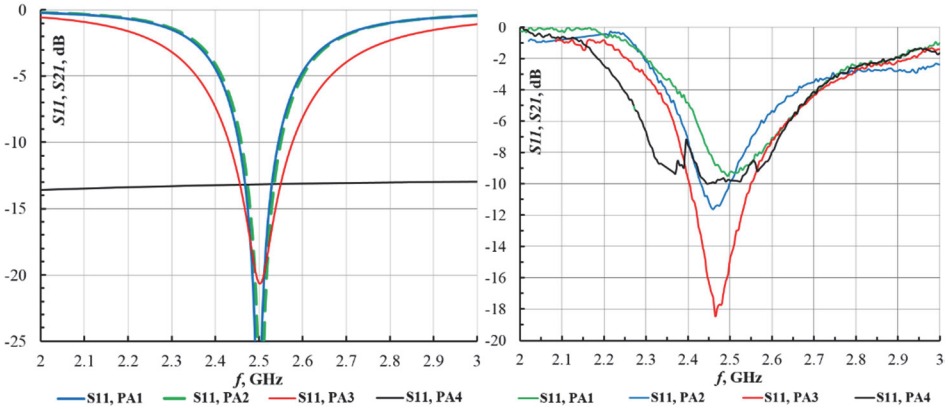


Fig. 3.3. Quad power amplifier chip *S*-parameter simulation and measurement results: (a) simulation results; (b) measurement results

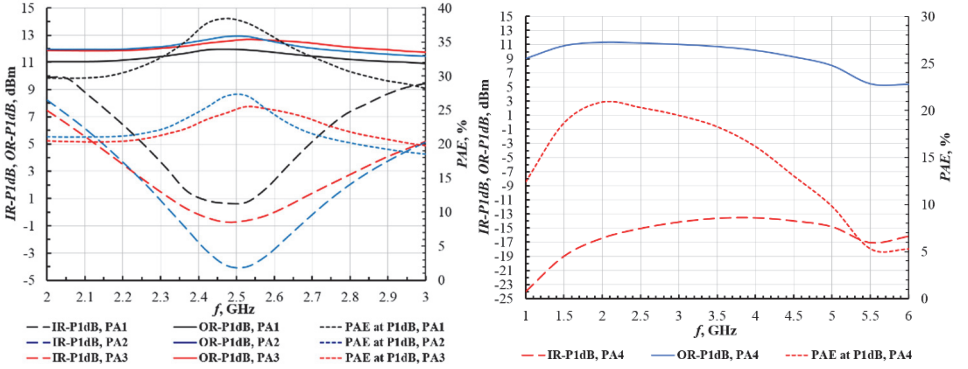
All four designed PAs are matched with a single impedance matching network at both the amplifier input and output for the widest bandwidth. Bondwires and parasitic bond-pad capacitances are also included in the simulations. Analyzing the results presented in Fig. 3.3a one can note that the widest simulated matching bandwidth is obtained when self-biased PA (PA4) configurations are utilized. Moreover, the gain of the self-biased PA is around 10 dB larger compared to other PAs due to better input matching S_{11} quality and the fact that the input stage also provides amplification. The second widest matched bandwidth (400 MHz at $S_{11} \leq -5$ dB) is obtainable using the cascode configuration with feedback (PA3). The carefully selected *RC* feedback circuit component values slightly increase the real part of the input impedance (in this case from around 4 Ω to around 12 Ω) which leads to a smaller impedance transformation ratio. The feedback circuit also makes both the real and imaginary parts of the input impedance constant over a wider bandwidth (around 100 MHz difference), compared to that without the feedback circuit. Cascode PA without

feedback (PA2) and a single transistor PA (PA1) have an identical S_{11} response which is around 300 MHz wide at $S_{11} \leq -5$ dB.

The gain for both cascode PAs as well as the single transistor PA are centered around the matched bandwidth minimum. The cascode PA without feedback provides maximum achievable gain of 17 dB at 2.5 GHz (which LTE B41 and is included in the existing mid-band 5G range), taking into account that all four designed PAs have a similar output power in the range of 12–13 dBm. The cascode PA with feedback has a smaller gain of 14 dB with the single transistor PA providing the smallest gain of 12 dB. The self-biased PA provides the largest simulated gain from 32 dB to 21 dB in the frequency range of 1 GHz to 6 GHz. This is due to the high simulated input impedance matching quality over the latter frequency range.

Small-signal *S*-parameter measurement results are presented in Fig. 3.3b. The matching curves for both cascode PAs as well as the single transistor PA resemble the simulated results. The cascode PA with feedback provides a matched bandwidth which is wider by about 70 MHz at $S_{11} = -5$ dB compared to the bandwidth of a cascode PA without feedback or to the single-transistor PA. The self-biased PA provides the largest matched bandwidth, although it doesn‘t cover the simulated band from 1 GHz to 6 GHz.

Large-signal harmonic balance (*HB*) simulation results are presented in Fig. 3.4. Input- and output-referred compression points are found at each of the simulated frequencies therefore Fig. 3.4 present the results of parametric sweep simulations.



(a) (b)

Fig. 3.4. Quad power amplifier chip harmonic balance simulation results: (a) single-transistor (PA1) and cascode with (PA2) and without (PA3) feedback power amplifier; (b) self-biased power amplifier (PA4)

Single-transistor (PA1), cascode PAs with (PA2) and without (PA3) feedback input- and output-referred compression points alongside with power added

efficiency values at the *P1dB* over different frequencies are presented in Fig. 3.4a. It is to be noted, that the frequency range for the latter PAs corresponds to the matched bandwidth. All PAs output a constant output power of around 12 dBm in the whole range, but the matching quality affects the gain. As the matching quality S_{11} reduces, the gain and *PAE* drop. The largest *PAE* is obtained using a single transistor PA, although its gain is the smallest. The cascode PA without feedback, on the other hand, provides the largest gain.

The same simulation results for cascode self-biased (PA4) amplifier are presented in Fig. 3.4b. Although the simulated matched bandwidth covers the whole 1 GHz to 6 GHz range, the *PAE* is sufficient to only around 4 GHz with a *PAE* of around 15%. The *PAE* reduces drastically at higher frequencies due to the reduced gain and output power level. Although the simulations in both Fig. 3.3a and Fig. 3.4b lead to believe that the self-biased PA architecture operating bandwidth is similar to that of a TWA, the measurement results presented in Fig. 3.3b reveal that the matched bandwidth is not as wide.

The amplifiers, included in the designed Quad-PA ASIC, have been also investigated in the unlicensed mid-band 5G range at a center frequency of 6.5 GHz. Large signal simulation results are presented in Table 3.1. Even though most amplifier simulated efficiency is above 20%, the *PAE* decreases almost two times at a 3 dB back-off.

Table 3.1. Quad power amplifier chip simulations at 6.5 GHz

	IR-P1dB, dBm	*OR-P1dB*, dBm	*PAE* at *P1dB*, %	*PAE* at 3 dB back-off, %
PA1	0.3	9.8	16.2	8.3
PA2	6.1	12.6	21.5	12.9
PA3	5.3	13.0	26.15	16.5
PA4	−2.5	12.0	27.0	16.8

The first step in testing the designed quad-PA ASIC is to compare the simulated and measured DC currents. The latter comparison is presented in Table 3.2. The single transistor PA (PA1) bias voltage is provided externally and the measurement results with three different bias voltages are presented in Table 3.2. The bias voltages for the cascode PAs (PA2 and PA3) are formed internally but require an external constant reference current I_{bias}. The DC current consumption for PA2 and PA3 with three different I_{bias} values is also presented in Table 3.2. Self-biased PA (PA4), on the other hand, contains an input stage with a fixed supply and, hence, current. Therefore, currents for only input and output stages are measured.

Based on the results presented in Table 3.2, the DC current for PA4 differs by 20% and can be a result of an error in the fabrication stage. The designed PA2 and PA3 are operating as intended, as the difference between the simulated and measured current consumption is less than 10%.

Table 3.2. Quad power amplifier chip current measurement summary

	PA1		PA2		PA3		PA4	
	I_{DC}	V_{bias}	I_{DC}	I_{bias}	I_{DC}	I_{bias}	$I_{DC,\ in.stg}$	$I_{DC,\ out.stg}$
Sim.	21 mA	700 mV	27 mA	500 µA	28 mA	500 µA	5.5 mA	23 mA
Meas.	16.4 mA		30 mA		29.5 mA		3.9 mA	19 mA
Sim.	48 mA	1 V	50.5 mA	1 mA	50.7 mA	1 mA	–	–
Meas.	42.1 mA		52 mA		52 mA		–	–
Sim.	66 mA	1.2 V	81 mA	1.8 mA	81 mA	1.8 mA	–	–
Meas.	56 mA		82 mA		82.2 mA		–	–

The output stage current consumption depends on the bias voltage formed in the input stage in PA4. Due to the lower input stage supply current, the output stage current differs from the simulated value by around 17%. This can be compensated by increasing the supply voltage of the PA4 input stage from 1.6 V to 1.8 V. Measurement results for the designed ASIC containing four independent PAs are presented in Table 3.3. All PAs have been measured at 2.5 GHz (an existing LTE band B41, included in the 5G mid-band range). The measured *IR-P1dB* and *OR-P1dB* correspond to the simulated results for all PAs except the single transistor one (PA1). The difference between the measured and simulated *PAE* is in the region of 0.5% to 2.7%.

An *Agilent E4432B* signal generator, 7 GHz bandwidth *Agilent N9010A* spectrum analyzer, *Keysight E3631A* laboratory power supply, *Agilent U3402A* bench multimeter, and a 6 GHz bandwidth *HP8753E* vector network analyzer have been used during the designed quad-PA ASIC measurements.

Different single-stage classical PA architectures have been designed and fabricated using a 0.13 µm CMOS process. The researched classical PA architectures include a single transistor PA, a cascode PA with and without feedback as well as a self-biased PA. Simulations and measurements at a center frequency of 2.5 GHz (an existing LTE band B41, included in the 5G mid-band range) revealed, that the achievable practical matched bandwidth can span to 400 MHz with a typical bandwidth of 300 MHz.

Table 3.3. Quad power amplifier chip output power and efficiency measurement summary

	f, GHz	*Classical PA type*	*IR-P1dB*, dBm	*OR-P1dB*, dBm	*PAE*, %
Sim.	2.5	Single transistor PA (PA1)	0.7	11.9	37.2
Meas.			0.5	5.5	10.1
Sim.		Cascode with feedback PA (PA2)	−4.0	13.0	27.1
Meas.			−2.5	12.0	25.7
Sim.		Cascode without feedback PA (PA3)	−0.9	12.2	25.0
Meas.			0	11.2	24.5
Sim.		Self-biased PA (PA4)	−15.0	11.1	20.0
Meas.			−18.0	8.6	17.3

The single transistor PA provides the largest (up to 35%) *PAE* with the smallest gain (around 10 dB) and a typical matched bandwidth of 200 MHz. The cascode PA with feedback provides a 300 MHz bandwidth and medium gain (around 14 dB) and practical *PAE* of around 25%. The cascode PA without feedback provides a 200 MHz bandwidth and high gain (around 17 dB) and practical *PAE* of around 25%. The self-biased PA provides the highest gain (around 25 dB) and widest matched bandwidth of around 400 MHz but the practical *PAE* is around 17%.

3.1.2. Traveling Wave Amplifier Architecture

The second designed ASIC contains two independent TWAs with the simplified schematics presented in Fig. 3.5 and the layout alongside the fabricated IC microphotograph given in Fig. 3.6.

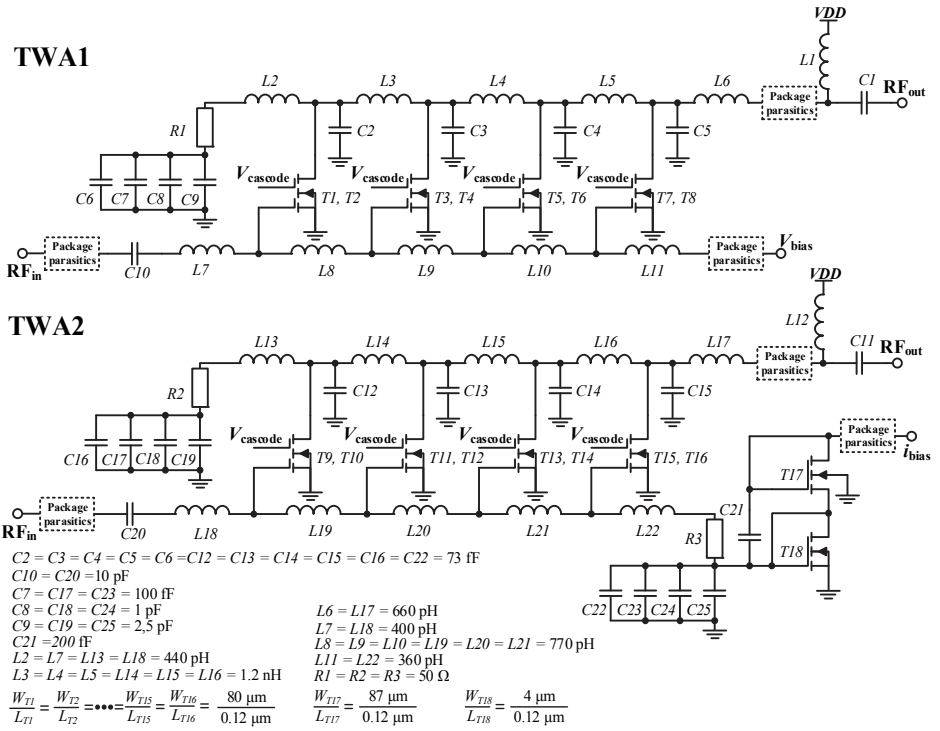


Fig. 3.5. *IBM* 0.13 µm CMOS Traveling wave amplifier chip simplified schematic

Both TWAs are identical except the gate bias and termination circuits. One TWA contains an integrated bias and RF termination circuit, the other one – with an external one. Both the gate and the drain termination circuits present a 50 Ω

load for AC signals but are an open circuit for DC. The series capacitance for termination resistors is formed by four different value capacitors in parallel in order to provide the lowest impedance to ground for different frequency signals.

The TWA itself contains four identical segments of cascode configuration transistors, which are shown in Fig. 3.5 as double gate NMOS devices. The input *LC* transmission line has been designed by adjusting the inductance to the 253 fF input capacitance for each of the four TWA segments. The latter input capacitors alongside with 770 pF inductors form an *LC* circuit with a corner frequency of 11.5 GHz.

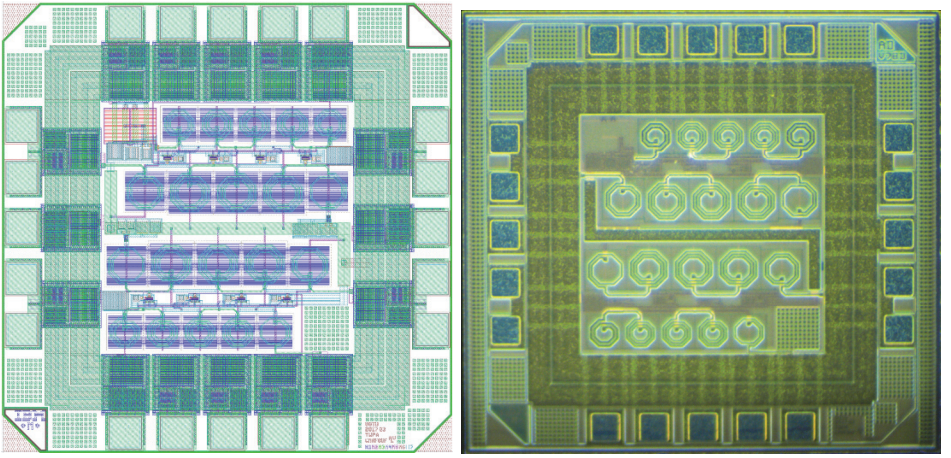
Additional 73 fF capacitors have been added in order to adjust the drain-source capacitance to a total of 280 fF and, in combination with L = 1.2 nH inductors, to achieve a corner frequency of 9.2 GHz. In both cases, the corner frequencies are calculated using Eq. (3.1):

$$f_{3\text{dB}} = \frac{1}{2\pi\sqrt{LC}}. \tag{3.1}$$

The initial drain and gate transmission line circuit inductors are calculated based on the shunt capacitance and the target corner frequency using Eq. (3.2):

$$Z_{\text{line}} = \sqrt{\frac{L}{C}}. \tag{3.2}$$

The estimated gate and drain inductor L values have been further optimized during the simulation stage in order to achieve the flattest gain response over the widest frequency range.



(a) (b)

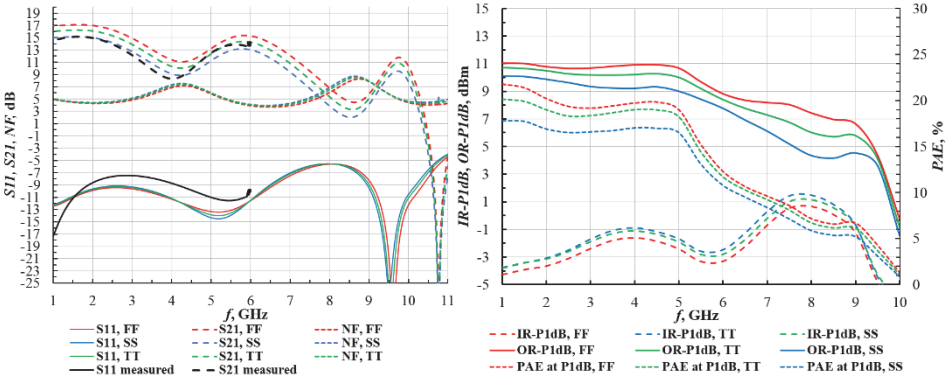
Fig. 3.6. *IBM* 0.13 μm CMOS traveling wave amplifier: (a) layout; (b) fabricated IC

The input of both TWAs are DC blocked using 10 pF capacitors. The input and output of both TWAs are connected to the package using double bondwires

in order to achieve a transmission line impedance closer to 50 Ω. The supply voltage for both designed TWAs is 1.6 V. V_{cascode} is used as gain control for both TWAs.

The designed TWAs are simulated under three operating condition sets: typical *TT* corner (40 °C operating conditions, typical NMOS and PMOS transistor parameter models), slow *SS* corner (80 °C operating conditions, worst-case fabricated NMOS and PMOS transistor parameter models) and fast *FF* corner (−40 °C operating conditions, best-case fabricated NMOS and PMOS transistor parameter models).

TWA with off-chip gate termination (TWA1) simulation results are presented in Fig. 3.7. Small-signal *S*-parameter simulation results under different operating corner conditions are presented in Fig. 3.7a. The TWA with an off-chip gate termination resistor operating bandwidth with $S_{11} \leq -5$ dB spans from 1 GHz to around 10.8 GHz. The S_{21} gain of is above 10 dB and a ±1 dB offset over different corners to around 7 GHz. The initial ideal model simulation results, on the other hand, revealed a flat gain response up to 10 GHz.The gain response is not flat as the termination resistor is connected through a single bondwire, which introduces reflections into the TWA gate transmission line. The noise figure *NF* is in the region from 5 dB to 7.5 dB up to 8 GHz and the shape of the curve follows the shape of the S_{21} gain curve. The stability curve is not presented as the stability factor $K_f > 6$ in the whole frequency region of interest. The nominal bias voltage for the designed TWA1 is $V_{\text{bias}} = 660$ mV.



(a) (b)

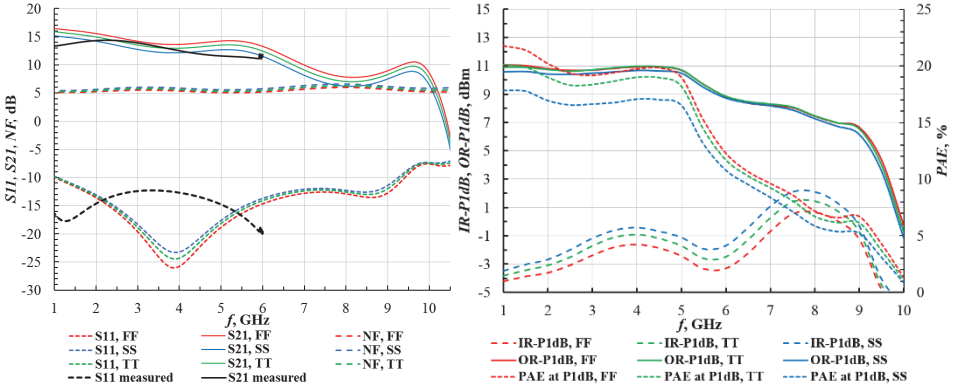
Fig. 3.7. Traveling wave amplifier chip simulation and measurement results: (a) TWA1 with off-chip termination gate *SP* simulation and measurement results; (b) TWA1 with off-chip gate termination *HB* simulation results

Large-signal harmonic balance simulation results over the full operating bandwidth at three corner conditions are presented in Fig. 3.7b. The average output-referred compression point (*OR-P1dB*) is around 11 dBm. The power

added efficiency (*PAE*) is equal to a classical *AB*-class PA up to around 5 GHz. The simulations were conducted with a constant 33 nH RF choke inductor. The latter inductor provides sufficient gain and therefore *PAE* up to 5 GHz. At higher frequencies, the gain of the transistor naturally reduces and therefore the *PAE* drops. In order to increase the *PAE* above 5 GHz, a smaller value inductor is required.

TWA with on-chip gate termination (TWA2) simulation results are presented in Fig. 3.8. Small-signal *S*-parameter simulation results under different operating corner conditions are presented in Fig. 3.8a and are similar to the results presented in Fig. 3.7a. The on-chip termination leads to a much flatter gain response, a better S_{11} value and lower noise levels over the frequency range of interest, compared to that of TWA2. Large-signal harmonic balance simulation results over the full operating bandwidth at three corner conditions are presented in Fig. 3.8b. The large-signal simulation results are similar for both TWA1 and TWA2 with a *PAE* value close to that of a classical PA and dropping below 20% at frequencies above 5 GHz. The TWA with an on-chip termination circuit is also unconditionally stable over the whole frequency range, therefore the stability factor K_f is not shown. The nominal bias current for the designed TWA2 is $I_{\text{bias}} = 550$ μA.

The designed TWAs were investigated at a center frequency of 6.5 GHz, included in the mid-band 5G range, using large signal harmonic balance simulations. The latter research revealed the following parameters: an *IR-P1dB* of −2.2 dBm, *OR-P1dB* of 8.2 dBm, a *PAE* at *P1dB* equal to 16.2% and a *PAE* at 3 dB back-off equal to 6.4%. Similar to the classical PAs, the TWA *PAE* also drops drastically below the amplifier compression point.



(a) (b)

Fig. 3.8. Traveling wave amplifier chip simulation and measurement results: (a) TWA2 with on-chip gate termination *SP* simulation and measurement results; (b) TWA2 with on-chip gate termination *HB* simulation results

An *Agilent E4432B* signal generator, 7 GHz bandwidth *Agilent N9010A* spectrum analyzer, *Keysight E3631A* laboratory power supply, *Agilent U3402A* bench multimeter, and a 6 GHz bandwidth *HP8753E* vector network analyzer have been used during the designed dual-TWA ASIC measurements.

The first step in testing the designed dual-TWA ASIC is to compare the simulated and measured DC currents. The latter comparison is presented in Table 3.4. The TWA with off-chip termination (TWA1) requires an external bias voltage to set the operating point for the amplifier, whereas TWA with an on-chip termination circuit (TWA2) requires a bias current.

Table 3.4. Traveling wave amplifier current measurement summary

	TWA1		TWA2	
	I_{DC}	V_{bias}	I_{DC}	I_{bias}
Sim.	36 mA	600 mV	36 mA	550 μA
Meas.	38.1 mA		37.7 mA	
Sim.	58.5 mA	800 mV	59.68 mA	1 mA
Meas.	59.3 mA		61.7 mA	
Sim.	90.75 mA	1 V	97.4 mA	1.8 mA
Meas.	92 mA		99.2 mA	

P1dB and *PAE* measurements at frequencies of 1 GHz, 2 GHz and 2.9 GHz for both designed TWAs are presented in Table 3.5. Summarizing the presented results, the manufactured TWAs performed 2.3% to 3.1% less efficient than simulated with the maximum overall *PAE* reaching 18%.

S-parameter measurement results are presented alongside simulation results in Fig. 3.7a and Fig. 3.8a. The overall shape of *S*-parameter responses for both TWAs differs from the simulated ones. The shape of the S_{21} gain response for TWA1 is close to simulated of *SS* corner condition, although the matching quality S_{11} response is worse due to the impedance mismatch in the off-chip gate termination resistor. The S_{21} gain response for TWA2 with on-chip gate termination is shifted to the lower frequency range maintaining the simulated curve shape. On-chip gate termination provides a better S_{11} response, compared to that of TWA1. This is due to the smaller impact of the bondwire on the RF input transmission line.

Table 3.5. Traveling wave amplifier output power and efficiency measurement summary

	TWA1				TWA2			
	f, GHz	*IR-P1dB*, dBm	*OR-P1dB*, dBm	*PAE*, %	*f*, GHz	*IR-P1dB*, dBm	*OR-P1dB*, dBm	*PAE*, %
Sim.	1.0	−3.3	10.6	20.3	1.0	−4.2	10.9	20.0
Meas.		−0.5	10.4	18.0		−4.8	10.2	17.5
Sim.	2.0	−2.1	10.5	19.7	2.0	−3.1	10.8	19.3
Meas.		−1.2	10.1	16.5		−4.1	9.9	16.2
Sim.	2.9	−1.9	10.2	19.0	2.9	−2.0	10.9	18.7
Meas.		−1.1	9.9	15.8		−2.3	9.8	15.9

The measured frequency ranges do not fully correspond to the simulated ones due to the signal generator range (up to 3 GHz) and the VNA range (up to 6 GHz). It is also to be noted, that the measured *S*-parameter curves contain noise at the supported bandwidth edge in Fig. 3.7a and Fig. 3.8a.

TWA is a promising architecture to be implemented in 5G networks due to its large operating bandwidth, suitable for all 5G frequency bands. Two TWAs have been implemented in a 0.13 μm CMOS process. The measurement results revealed that the on-chip gate termination circuit leads to smaller losses and better performance compared to when the termination is off-chip. The designed TWAs provided a typical gain of around 14 dB with a matched bandwidth of 10 GHz. On the other hand, the measured *PAE* at *P1dB* is similar to that of classical PAs and is around 16% over the bandwidth. The latter characteristic is further reduced at lower input signal power levels (with relation to the TWA *P1dB* compression point) and does not suffice the aim of ensuring a network of efficient battery powered devices.

3.2. Doherty Power Amplifier Design

Chapter 2 of this dissertation provides a comparison between currently available advanced RF PA architectures – ET/EER PA, TWA, DPA, outphasing and mm-wave PAs. The previous chapter, Chapter 3.1, presents simulation and measurement results for different classical PA architecture variations and two types of TWA designs. The classical PA architecture can provide sufficient *PAE* but only working at the compression point, which is not always the case. Moreover, classical CMOS PAs can only be designed to cover a wide frequency range (in the order of an octave bandwidth) only at certain output power levels. This is due to the size of the power transistor, which determines the input impedance. At higher output powers, the CMOS power transistor impedance varies over frequency greatly, therefore reducing the matched bandwidth to around 200–400 MHz with a condition of $S_{11} \leq -10$ dB. The TWA, on the other hand, can provide a wide matching bandwidth (more than an octave) at various output power levels, but the *PAE* is comparable to that of the classical PA. ET/EER PAs has a bottleneck in the modulator bandwidth which directly affects the IF bandwidth and currently can't cope with the expected 5G network IF bandwidths above 150 MHz. The theoretical model of outphasing PAs is attractive due to its high efficiency, although both practical bandwidth and efficiency are far from ideal and are difficult to obtain. Millimeter wave PAs usually work at tens of gigahertz and, therefore, usually employ either the simplest classical architecture or sometimes DPA approaches. DPAs, on the other hand, provide sufficient efficiency over a wide input power range and can be

implemented using both on-chip, lumped and distributed parameter components. Moreover, DPAs are not subjected to IF bandwidth restrictions.

Therefore, DPA is the most attractive advanced PA architectures for future 5G wireless network devices. Two types of DPAs with design stages and simulation results are discussed in the following subsections. Chapter 3.2 is concluded with a quantitative comparison of the two designed DPA architecture variations.

3.2.1. Doherty Power Amplifier Target Specification

Two DPA architecture variations presented in the following subsections and have been designed to be compliant with mid-band 5G requirements (frequency and output power). The summarized target specifications are presented in Table 3.6.

Table 3.6. Doherty power amplifier target specifications

Parameter name	Target value/Comment
Target frequency	6.5 GHz
Operating bandwidth (unlicensed mid-band 5G)	5.9–7.1 GHz
IF bandwidth	≥150 MHz
Output power	15–24 dBm
Power gain	5–10 dB
Stability	Unconditionally stable
Back-off power	3–6 dB
Power added efficiency	25–35% at back-off power
Source/load impedance	50 Ω
Layout area	<1 mm^2
Technology	*TSMC* 0.18 μm RF CMOS

The latter band is selected due to a new concept in wireless radio frequency communication, where spectrum sharing is included. This means, that 3GPP introduces unlicensed bands in the wireless communications industry, which usually incorporates only licensed bands. As a result, the selected 5.9–7.1 GHz band can bind the new radio (NR) concept with the existing technology, resulting in NR/NR, NR/LTE and NR/*Wi-Fi* communications (Qualcomm Technologies Inc., 2017).

The configuration of the DPA must be determined before designing its individual components. This includes determining the classes of both PAs and whether or not they supply the same maximum current (identical or different geometry), the input signal power splitting ratio and the type of power splitter used, as well as the output impedance inverter configuration.

The main goal of this dissertation is to conduct research on whether the DPA with a simplified output impedance inverter configuration provides comparable specifications to those of the classic configuration. The DPA shall consist of a

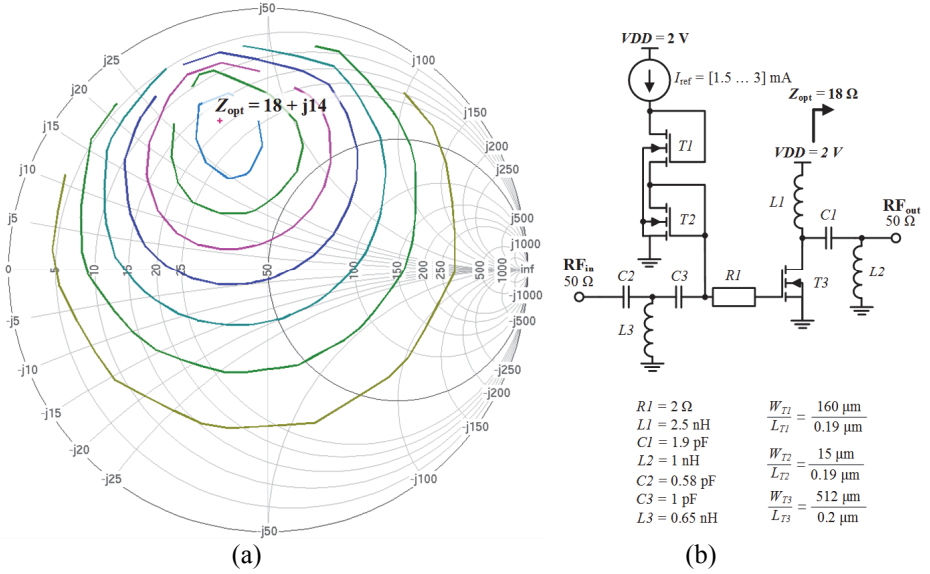
linear biased *AB*-class PA, a nonlinear *C*-class biased PA with identical geometry and an equal input signal power splitting ratio.

The following subsections discuss the whole design process an *ABC*-class DPA with both classic and simplified output impedance inverters.

3.2.2. Linear Power Amplifier Design

The first step in designing a DPA is to create the linear power amplifier (Fig. 3.9). The output operating voltage region of the NMOS transistor is limited by the knee and the breakdown voltages. The optimum load resistance R_{opt} for a given RF output power P_{OUT} and supply voltage V_{DD} is approximated by Eq. (3.3):

$$R_{opt} \approx \frac{V_{DD}^2}{2 \cdot P_{OUT}}. \tag{3.3}$$



(a) (b)

Fig. 3.9. Linear power amplifier: (a) Smith chart with constant output power contours; (b) simplified schematic

An output power of 20 dBm (84 mW) has been chosen as the target and is in the middle of the provided specification power region in Table 3.5, bearing in mind that the simulated output power will be lower due to the transistor model parasitic parameters including the knee voltage. Given the supply voltage of 2 V, the resulting optimal load resistance is $R_{opt} = 24\ \Omega$.

The maximum output current I_{max}, supplied by the transistor, defines its geometry as well as the bias point and is equal to 167 mA according to Eq. (3.4):

$$I_{\max} = 2 \cdot I_{\mathrm{DC,lin}} \approx \frac{2 \cdot V_{\mathrm{DD}}}{R_{\mathrm{load}}}. \tag{3.4}$$

A-class linear PA has been chosen, therefore the NMOS bias point is set for the transistor to constantly drain 83.5 mA.

The optimal load resistance, approximated using Eq. (3.3), is further corrected taking into account the parasitic parameters of the transistor model in the *TSMC* 0.18 µm RF CMOS process libraries. This is done via *Cadence ADE Load-pull* simulation. The results of the latter simulation are constant output power contours on a Smith chart, presented in Fig. 3.9a. The output power is constant in each point of the swept load impedance on the contour, but differs from contour to contour. The inner contours refer to less output power and the closer the contour is to the optimum load impedance, the higher the output power. The maximum output power is simulated at the load impedance of $Z_{\mathrm{opt}} = 18 + j14$ and slightly differs from the results acquired using Eq. (3.3). The latter impedance is matched to 50 Ω and using an impedance matching network. The output impedance matching network has been calculated using *IMNS Toolbox* plug-in, discussed in Chapter 2 of this dissertation and results in C_1 and L_2 components with the values given in Fig. 3.9b.

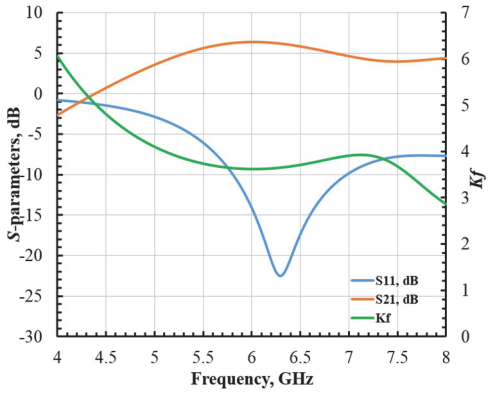
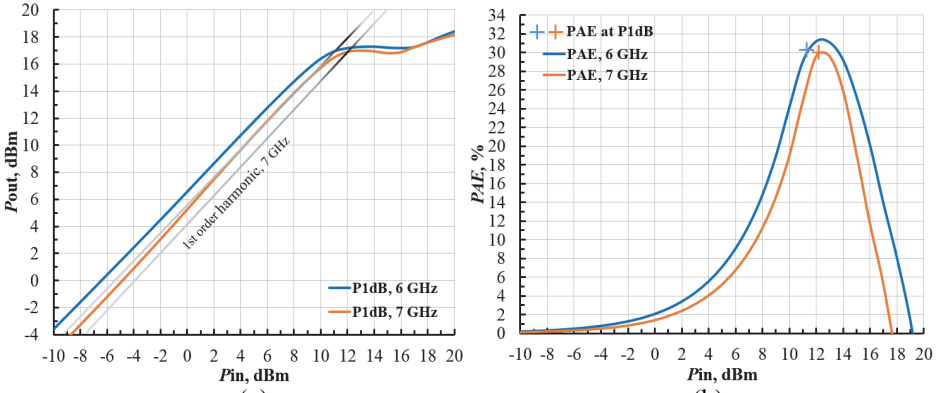


Fig. 3.10. Linear power amplifier small-signal *S*-parameter simulation results

The next stage of designing any linear PA is matching the input to the source impedance (in this case $Z_{\mathrm{S}} = 50\ \Omega$). The *T*-type input impedance matching network has also been designed using *IMNS Toolbox* plug-in with the component values presented in Fig. 3.9b.

The designed linear PA small-signal *S*-parameter simulation results are presented in Fig. 3.10. According to the latter figure, the PA: is unconditionally stable ($K_f > 1$) in the frequency range from 4 GHz to 8 GHz; is matched to the range from 5.8 GHz to 7 GHz with $S_{11} \leq -10$ dB; and an average gain of 6 dB in

the same region. The initial target gain for the 6–7 GHz frequency range was around 10 dB, but simulations revealed that only 6 dB to 7 dB is achievable using *TSMC* 0.18 μm RF CMOS.



(a) (b)

Fig. 3.11. Linear power amplifier harmonic balance simulation results: (a) 1 dB compression curves; (b) power added efficiency curves

Small-signal simulation is followed by large-signal simulation – harmonic balance with the *P1dB* compression and the power added efficiency (*PAE*) curves presented in Fig. 3.11. Two corner frequencies in the target range have been selected in order to evaluate the performance of the designed linear PA. The 1 dB output-referred compression point (*OR-P1dB*) is 17 dBm with a power gain of around 5 dB at both 6 GHz and 7 GHz with the *PAE* at *P1dB* of around 30%.

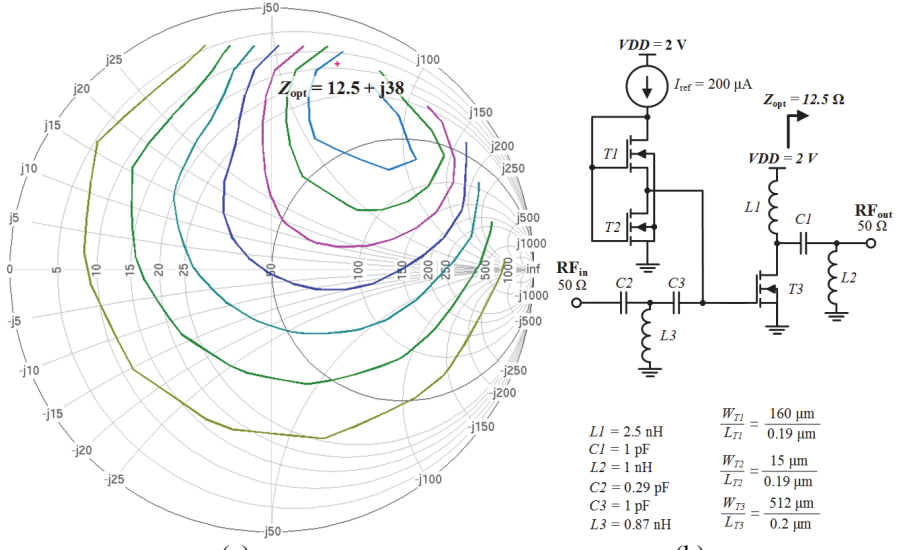
This results in an unconditionally stable *AB*-class linear PA matched to a frequency range of 6–7 GHz with an average power gain of 5 dB, an output power of *P1dB* = 17 dB and a *PAE* at *P1dB* of around 30%.

3.2.3. Nonlinear Power Amplifier Design

The second step in designing a DPA is to create a nonlinear PA. The design process is similar to that of the linear PA and starts with determining the size of the transistor.

Due to the initial statement, that both PA types will be of the same geometry, hence output current, the NMOS width and length are identical to those shown in Fig. 3.9b. The only difference is the bias circuit configuration, which provides a subthreshold voltage of around 200 mV with a reference current of 200 μA and setting a *C*-class operating point for the NMOS transistor. After determining the bias circuit and the PA geometry the optimal load must be found using load-pull

simulation with the resulting constant output power circles presented in Fig. 3.12a.



(a) (b)

Fig. 3.12. Nonlinear power amplifier: (a) Smith chart with constant output power contours; (b) simplified schematic

The optimal load impedance has been found to be $Z_{opt} = 12.5 + j38$ and the output impedance matching network, designed using the created *IMNS Toolbox*, presented in Fig. 3.12b.

Matching the input to the source impedance (in this case $Z_S = 50\ \Omega$) is done in the same way as with the linear PA. The *T*-type input impedance matching network has been designed using *IMNS Toolbox* plug-in with the component values presented in Fig. 3.12b. The designed nonlinear PA small-signal *S*-parameter simulation results are presented in Fig. 3.13. According to the latter figure, the PA is unconditionally stable ($K_f > 1$) in the frequency range from 4 GHz to 8 GHz, is matched to the range from 6.2 GHz to 7 GHz with $S_{11} \leq -10$ dB. The small-signal gain S_{21} is not presented in the latter figure due to the nature of operation of the *C*-class PA – the correct operation of the *C*-class PA is displayed using large signal simulation conditions.

Fig. 3.14 presents large-signal harmonic balance simulation results – the compression and power added efficiency curves at corner frequencies. The compression point at both 6 GHz and 7 GHz is higher than 20 dBm and is not displayed in Fig. 3.14a, but this is not required as the gain of the *C*-class PA is close to that of an analog buffer. At 6 GHz the *C*-class PA starts amplifying at around 5 dBm input power and to around 14 dBm with a power gain of around

4.5 dB. The *PAE* in this input power region is higher than 30%. At 7 GHz, the point at which the PA starts amplifying shifts to 8 dB with the same power gain and more than 25% *PAE*.

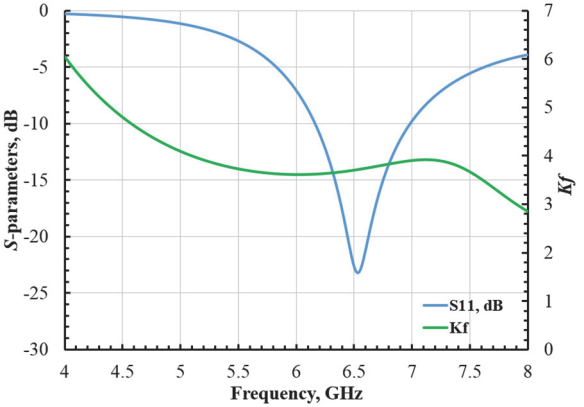
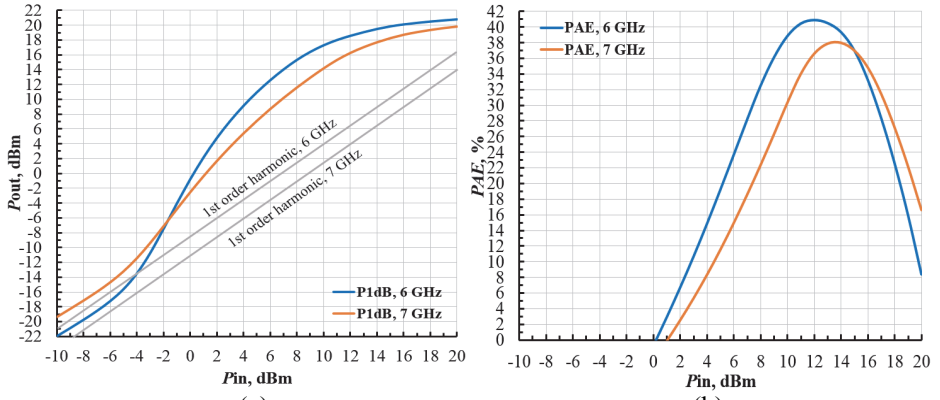


Fig. 3.13. Nonlinear power amplifier small-signal *S*-parameter simulation results

The nonlinear PA is designed in such a way, that it turns on and starts amplifying when input signals reach levels when the linear PA starts compressing – at inputs signal power levels of around $P_{\text{nonlinear,ON}} = P1dB_{\text{linear}} - 3$ dBm.



(a) (b)

Fig. 3.14. Nonlinear power amplifier harmonic balance simulation results: (a) 1 dB compression curves; (b) power added efficiency curves

That way, the nonlinear PA gain compensates for the linear PA compression and extend the linear operation with high *PAE* in a wider input power range (3 dB, 6 dB or even 10 dB back-off powers can be found in the state of the art published DPA articles).

3.2.4. Doherty Power Amplifier With a Classical Impedance Inverter Design

The classical DPA configuration contains the following building blocks: input power splitter, two differently biased PAs and an output impedance inverter. The output impedance inverter is the main component, which distinguishes the DPA from other PA architectures and is the main area of research in this dissertation. An idealized equal input power splitter was used in the simulations, but an additional 0.5 dB transmission loss has been included for the results to better match practical solutions. In general, the input power splitter can be either hybrid or Wilkinson in both even and uneven power splitting ratio depending on the levels at which both PAs saturate. The linear (later referred as the carrier) and the nonlinear (later referred as the peaking) PAs have been designed and presented with component values in Fig. 3.9 and Fig. 3.12. The only thing that is excluded from the latter PAs is the output matching networks (C_1 and L_2 components) as the outputs are matched to different load impedances.

The designed DPA with the classic output impedance inverter elaborated is presented in Fig. 3.15.

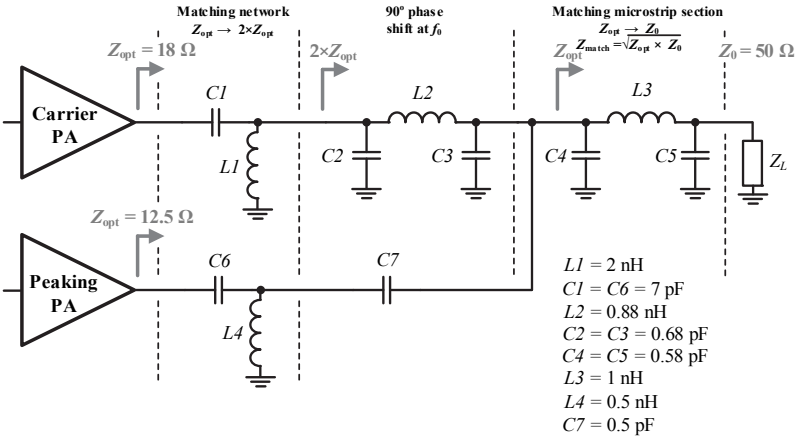


Fig. 3.15. Classical Doherty power amplifier impedance inverter arrangement

The designed carrier PA has an optimal load impedance of $Z_{opt,\ carrier} = 18\ \Omega$, whereas the peaking PA has an optimal load impedance of $Z_{opt,\ peaking} = 12.5\ \Omega$. Both of these PAs are matched to a microstrip line with an impedance of twice as large to that of $Z_{opt,\ carrier}$. Capacitor C_7 is used as a DC block, but its value also affects the compression point of the peaking PA. The phase shifting microstrip transmission line can be either lumped or distributed. In the case of a lumped microstrip line, it is presented as an equivalent $C_2L_2C_3$ π-type circuit with the values of the components calculated according to

$$L = \frac{Z_0}{2\pi f_0} \text{ and} \tag{3.5}$$

$$C = \frac{1}{2\pi f_0 Z_0}, \tag{3.6}$$

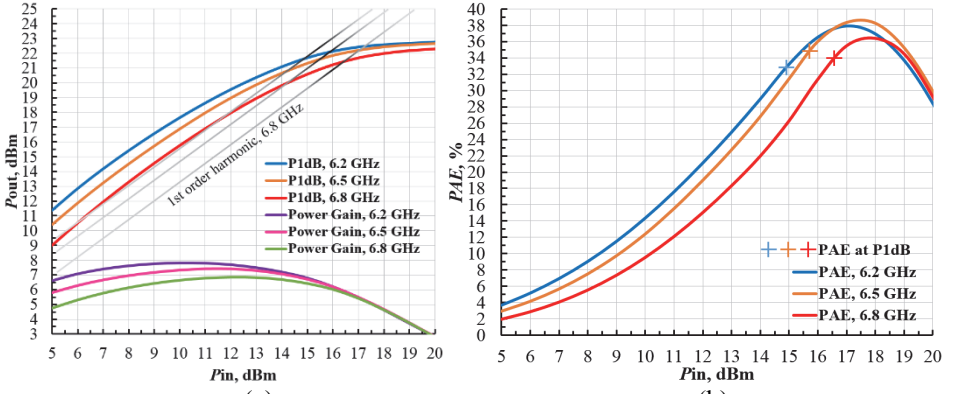
where C and L are lumped microstrip transmission line component values, Z_0 is the required impedance at f_0 target frequency.

The last element in the DPA is the matching microstrip transmission line $C_4L_3C_5$ π-type circuit which is used to match $2 \cdot Z_{\text{opt, carrier}}$ to the $Z_{\text{load}} = 50\ \Omega$ load impedance. The equivalent lumped component values are also calculated using Eq. (3.5) and Eq. (3.6), but the impedance of the matching Z_{match} section is found using

$$Z_{\text{match}} = \sqrt{Z_{\text{opt}} \times Z_{\text{load}}}\ . \tag{3.7}$$

Parallel capacitors C_3 and C_4 have been reduced to a single capacitor during the optimization stage, but these schematic optimizations have to be taken into account during the layout phase.

The overall performance of any DPA can be split into two phases: low and high power operating modes. During low power mode, the carrier PA is the only one operating and the peaking PA is off. As a result, the carrier PA output "sees" an impedance equal to the double optimal load impedance. As the carrier PA starts to compress, the peaking PA turns on and modulates the impedance "seen" by the linear PA thus extending the overall linear operating region of the DPA.



(a) (b)

Fig. 3.16. Classical Doherty power amplifier harmonic balance simulation results: (a) 1 dB compression and power gain curves; (b) power added efficiency curves

Classical DPA large signal harmonic balance simulation results are presented in Fig. 3.16. The *OR-P1dB* compression points at corner frequencies of 6.2 GHz

and 6.8 GHz, as well as the center frequency of 6.5 GHz, are 21.5 dBm, 20.4 dBm and 21.7 dBm accordingly with *PAE* above 33%. The bias current for the carrier PA is set to be 2.5 mA and 0.2 mA for the peaking PA, overall setting the DPA to high power mode. The overall DPA power gain in the 6.2 GHz to 6.8 GHz frequency range varies from 5 dB to 8 dB.

When the carrier PA bias current is reduced to 1.5 mA and the peaking PA current left unchanged, the DPA goes into low power mode – the *P1dB* and their *PAE* curves presented in Fig. 3.16b are shifted 3 dBm lower on the horizontal axis. As a result, the output power is reduced but the low power mode is intended to work with lower input powers at higher *PAE*. The aggregate DPA *PAE* curve at the center frequency of 6.5 GHz is presented in Fig. 3.17.

Taking into account that the DPA compresses at around 15.5 dBm in high power mode (HP), both low (LP) and high (HP) power configurations enable the designed DPA with the classical output impedance inverter to operate at *PAE* levels of more than 28% at 3 dB back-off at a center frequency of 6.5 GHz with a peak *PAE* of 38%.

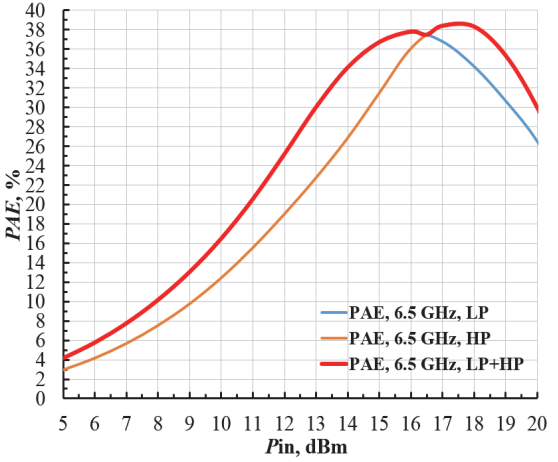


Fig. 3.17. Classical Doherty power amplifier configuration aggregate power added efficiency curve at 6.5 GHz

The layout of the DPA with the classical output impedance inverter is presented in Fig. 3.18. The overall area of both PAs and the impedance inverter is similar and the total occupied chip space is 0.722 mm^2. The input power splitter is not included in the DPA layout as it can be either on-chip or off-chip.

DPA architecture poses challenges in order to fine-tune the performance in practice therefore variable length delay lines are included. This way the phase of the splitted input signal can be fine-tuned after the DPA is fabricated and the best

performance conditions are found. The latter is the reason for not including the input power splitter in the internal layout.

The output of the DPA is connected to the package via bondwires and their impact on the performance can be reduced by addressing the latter connection as a lumped *CLC* transmission line.

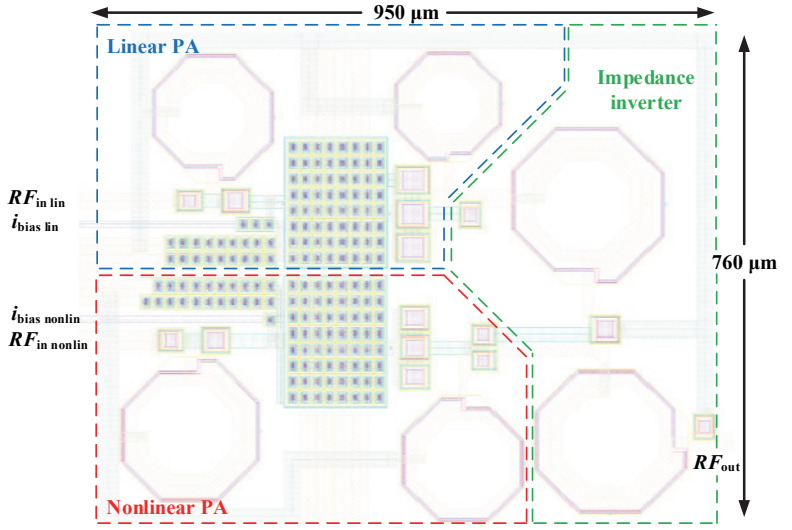


Fig. 3.18. Classical Doherty power amplifier configuration layout

With careful consideration of these values (possibly using double bondwires to reduce the inductance), it is possible to reduce the reflections in the RF transmission chain.

3.2.5. Doherty Power Amplifier With a Simplified Impedance Inverter Design

The DPA with a simplified impedance inverter (Lajovic, 2013) is presented in Fig. 3.19 and is similar to that in Fig. 3.15. The major difference is the absence of the matching microstrip impedance line. The carrier and the peaking PAs in this case are matched to a microstrip line with an impedance of $2{\cdot}Z_{load}$ and not to $2{\cdot}Z_{opt,carrier}$. Therefore, at low power modes the carrier PA "sees" a double load impedance in the same way like the DPA with a classical impedance inverter.

In the high power region, the peaking PA modulates the load and the DPA with a simplified impedance inverter operating range is extended similarly to that of the DPA with a classical impedance inverter. The lumped microstrip line component values are found using the same Eq. (3.5) and Eq. (3.6).

Simplified DPA large signal harmonic balance simulation results are presented in Fig. 3.20. The *OR-P1dB* compression points at corner frequencies of 6.2 GHz and 6.8 GHz as well as the center frequency of 6.5 GHz are 21 dBm, 20 dBm and 19.5 dBm accordingly with *PAE* around 30%.

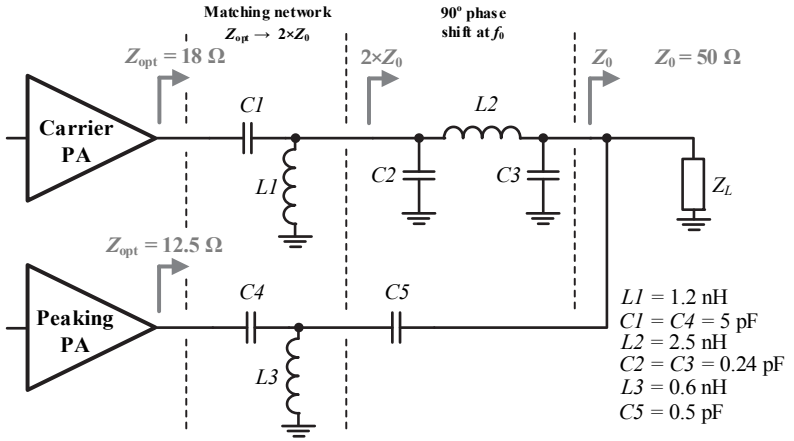
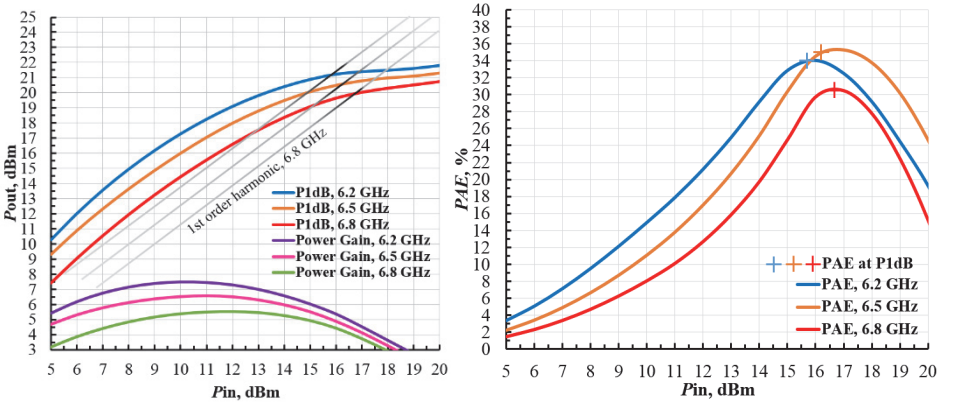


Fig. 3.19. Simplified Doherty power amplifier impedance inverter arrangement

The bias current for the carrier PA is set to be 3.5 mA and 0.2 mA for the peaking PA, overall setting the DPA to high power mode. The overall DPA power gain in the 6.2 GHz to 6.8 GHz frequency range varies from 5 dB to 7 dB. The results differ slightly compared to the ones presented for the classical DPA due to the larger impedance conversion ratio and the absence of the additional matching microstrip line segment.



(a) (b)

Fig. 3.20. Simplified Doherty power amplifier harmonic balance simulation results: (a) 1 dB compression and power gain curves; (b) power added efficiency curves

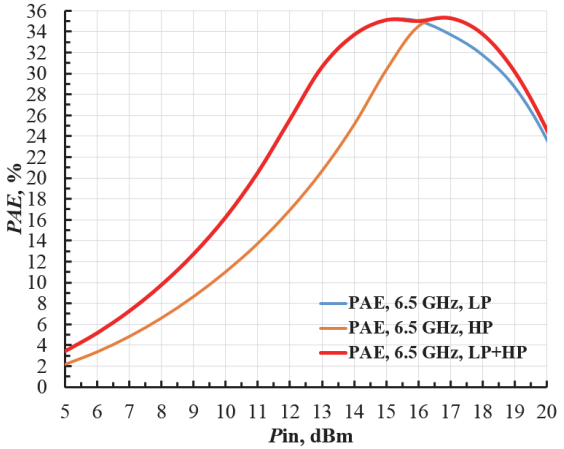


Fig. 3.21. Simplified Doherty power amplifier configuration aggregate power added efficiency curve at 6.5 GHz

This mainly affects the gain at different corner frequencies but is a compromise to be taken in order to reduce the layout area buts still maintain DPA features. When the carrier PA bias current is reduced to 2.5 mA and the peaking PA current left unchanged, the DPA goes into low power mode – the *P1dB* and their *PAE* curves presented in Fig. 3.20 are shifted 3 dBm lower on the horizontal axis. As a result, the output power is reduced but the low power mode is intended to work with lower input powers at higher *PAE*.

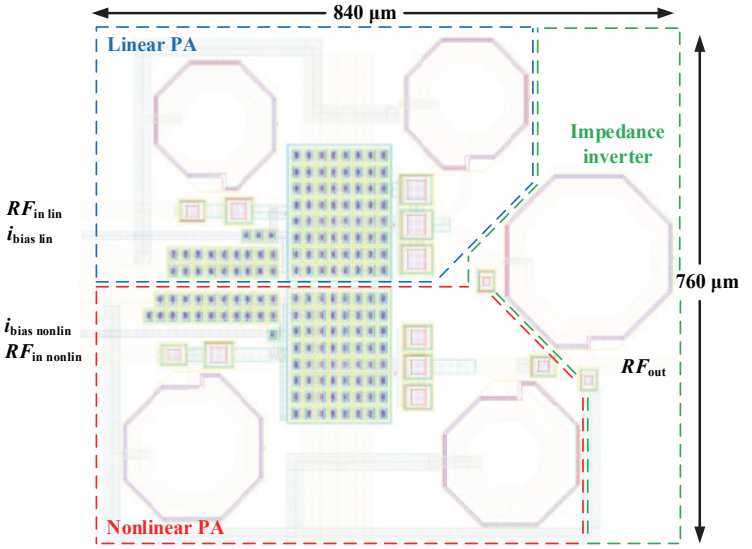


Fig. 3.22. Simplified Doherty power amplifier configuration layout

The aggregate DPA *PAE* curve at the center frequency of 6.5 GHz is in Fig. 3.21. Taking into account that the DPA compresses at around 15 dBm in high power mode (HP), both low (LP) and high (HP) power configurations enable the designed DPA with the classical output impedance inverter to operate at *PAE* levels of more than 26% at 3 dB back-off at a center frequency of 6.5 GHz with a peak *PAE* of 35%. This is 2% less at back-off power and 3% less peak *PAE* compared to the classical DPA configuration.

The layout of the DPA with the simplified output impedance inverter is presented in Fig. 3.22. The overall area of both PAs and the impedance inverter is similar and the total occupied chip space is 0.639 mm^2. The DPA with a simplified output impedance inverter occupies around 12% less space compared to the classical DPA configuration. Therefore, this type of DPA can be used when a DPA is intended to be integrated into a multifunctional transceiver where the less occupied silicon area means more possibilities for additional functionality.

3.2.6. Classical and Simplified Doherty Power Amplifier Configuration Comparison

Both classic and simplified DPAs provide sufficient *PAE* in the 6.2 GHz to 6.8 GHz frequency region and is suitable for the up-and-coming mid-band 5G devices. The simplified DPA provides around 3% smaller *PAE* at 6.5 GHz compared to that of the classic DPA but occupies 12% less area and therefore can become a compromise when silicon area is crucial.

Both designed DPAs are summarized and compared to the target specifications in Table 3.7.

Table 3.7. Classical and simplified DPA configuration parameter summary

Parameter name	Target value/ Comment	Classical DPA configuration	Simplified DPA configuration
Target frequency	6.5 GHz		
Operating bandwidth	5.9–7.1 GHz	6.2–6.8 GHz	
IF bandwidth	≥150 MHz	600 MHz	
Output power	15–4 dBm	21 dBm	20 dBm
Power gain	5–10 dB	6–8 dB	5–7 dB
Stability	Unconditionally stable		
Back-off power	3–6 dB	3 dB	
Power added efficiency	25–35% at back-off power	28% at back-off; 38% peak	26% at back-off; 35% peak
Source/load impedance	50 Ω		
Layout area	<1 mm^2	0.722 mm^2	0.639 mm^2
Technology	*TSMC* 0.18 μm RF CMOS		

Table 3.8. The designed DPA comparison to the state of the art amplifiers

Ref./architecture	Process	*VDD*, V	*f*, GHz	P_{linear}, dBm	Overall *PAE*, %	Back-off, dB
(Cui, Roblin et al., 2007)	0.18 µm CMOS	3.7	3.5	24.4	36.1	6
(Ryu, Jung & Jeong, 2012)	0.18 µm CMOS	3.3	2.4	29.5	22	5
(Kim, Son et al., 2014)	0.18 µm CMOS	–	0.89	25	43.6	5
(Ryu, Jang et al., 2014)	0.13 µm CMOS	3.3	2.4	31.9	30.1	5
This work						
Classical	0.18 µm CMOS	2	6.5	21	38	3
Simplified				20	35	

The designed DPA parameters are summarized and compared to those presented in the similar CMOS process scale in Table 3.8. Both designed DPA configurations are on par with the published DPAs, but is designed to operate at a much higher 6.5 GHz frequency with a smaller supply voltage. Although *TSMC* 0.18 µm RF CMOS process provides MOS devices which lack high gains at 6.5 GHz frequencies, it is possible to employ such a mature cost-efficient process, add pre-amplification stages to increase the gain and design RF DPAs suitable for 5G networks.

3.3. Third Chapter Conclusions

Research results presented in Chapter 3 address dissertation problem No. 1, raised in Chapter 1 conclusions section. Chapter 3 can be summarized with the following concluding statements:

1. A classical PA alongside with the TWA architectures are least suitable for the up-and-coming 5G wireless networks. Even though classical linear PAs are the base for advanced PA architectures, they lack sufficient *PAE* in CMOS process. The TWA provides more than an octave operating bandwidths, but, similarly to the classical PA, lack sufficient *PAE*. Several configurations of classical PAs integrated into a single ASIC have been designed using *IBM* 0.13 µm CMOS process, revealing that the practical *PAE* is around 20% at the compression point. Two types of TWAs integrated into an ASIC based on *IBM* 0.13 µm CMOS process were designed, revealing a matched bandwidth of around 10 GHz but a practical *PAE* similar to that of the classical PA – around 16% at the compression point. Both classical PA and TWA do not provide sufficient *PAE* at other operating points below their compression. Taking into account that 5G devices can operate at different power levels, the DPA might

provide the required efficiency at a broader span of output power levels.

2. DPA is the most promising PA architecture to be implemented in 5G wireless transmitters and transceivers due to the high achievable *PAE* at a wide input power range. Moreover, despite the fact that the DPA consists of multiple parallel PAs, it can be characterized as a single unit and therefore DPD techniques can be applied for additional linearization. The DPA is also one of the two advanced PA architectures alongside with TWA, which can be found in mm-wave PAs bearing in mind, that 5G networks are planned to have bands above 20 GHz.

3. Two DPA configurations have been investigated in this dissertation – one with a classical and one with a simplified output impedance inverter. Both DPAs have been designed in *TSMC* 0.18 μm CMOS and provide sufficient *PAE* in the 6.2 GHz to 6.8 GHz frequency region and are suitable for the mid-band 5G devices. The simplified DPA provides around 26 % at 3 dB back-off power and a peak 35% *PAE*, which is 3% smaller at 6.5 GHz compared to that of the classic DPA. But the slight reduction in *PAE* comes with the simplified DPA occupying 12% less area and therefore can become a compromise when silicon area is crucial therefore is a possible choice for 5G transmitters and transceivers operating in the mid-band frequency range with various output power levels including the lower power region (0.5 W and below).

General Conclusions

1. A qualitative and quantitative approach of characterizing envelope tracking, outphasing, TWA and Doherty advanced power amplifier architectures, has been proposed and can be used to define the adaptability of different CMOS nodes when designing low-, mid- and high-band 5G wireless transmitters ant transceivers.
2. The classical linear PA and TWA architectures have been designed and investigated in the mid-band 5G range (at 2.5 GHz and 6.5 GHz center frequencies) using *IBM (GlobalFoundries)* 0.13 μm deep submicron CMOS process, revealing a maximum 25% practical *PAE* at different input signal power levels and a matched bandwidth of up to 400 MHz and larger than one octave accordingly.
3. Two DPAs, one with a classical and the other with a simplified output impedance inverter, have been designed and investigated using *TSMC* 0.18 μm deep submicron CMOS process, revealing a larger than 25% *PAE* at 3-dB back-off, and a 38% peak *PAE* at 6.5 GHz input signal power levels, and the DPA with a simplified output inverter reducing the chip area up to 12%.
4. Taking into account, that the existing published impedance matching network design methods only include the equivalent series resistance, a

novel mathematical model and IMNS algorithm have been proposed, which take into account lumped component parasitic parameters reducing the largest offset of the S_{11} curve minimum to 1–7% when 0402 size 10% tolerance components are used.

5. In order to reduce the time and cost of designing power amplifier impedance matching networks only the most sensitive to change lumped surface-mount component, which affects the matching S_{11} response, needs to be high precision (less than or equal to 5%) while all other component tolerances can be kept lower, according to the IEC/EN 60062 standard.

6. The proposed novel IMNS algorithm and mathematical model have been implemented in a *IMNS Toolbox* plugin as a parto of a professional integrated circuit design software *Cadence Virtuoso*, reducing the number of simulation and measurement cycles to 1 when the frequency range is 1 MHz – 1 GHz and 1–3 iteration in the range from 1 GHz to 3 GHz.

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Summary in Lithuanian

Įvadas

Problemos formulavimas

Pastaraisiais metais, perėjimas nuo jau išvystytų 4G tinklų į besivystantį 5G belaidžio ryšio standartą kelia naujų iššūkių bei atveria naujų mokslinių tyrimų galimybių aukštadažniuose ir milimetrinių bangų grandynuose. Besivystantis 5G belaidžio ryšio standartas kelia aukštus reikalavimus ir galios stiprintuvams (GS): išėjimo galią nešiojamiems įrenginiams numatoma apriboti iki 24 dBm, efektyvumo lygį siekiama priartinti prie didžiausio teorinio tiesiniams GS pasiekiamo 50 % bei praplėsti veikimo dažnių diapazoną (Pham et al., 2017).

Belaidžio ryšio GS yra vienas iš daugiausiai galios sunaudojančių elementų siųstuvų grandynuose, todėl jo veikimo efektyvumas tiesiogiai įtakoja ir viso siųstuvo ar sistemos efektyvumą. GS, stiprinantis moduliuotus įėjimo signalus, veikia iki 12 dB žemiau soties taško, priklausomai nuo signalo moduliacijos tipo. Šiose sąlygose GS efektyvumas gali būti net 2 kartus prastesnis už įsotinto GS efektyvumą, o tai sąlygoja trumpesnius nešiojamų įrenginių veikimo laikus. Kadangi naujos kartos 5G tinklas sujungia daugybę įrenginių tarpusavyje ir numatoma, kad kiekvienas įrenginys gali būti daugiakanalis siųstuvas-imtuvas (angl. massive MIMO), bendras visos sistemos energijos suvartojimas tampa aktualia problema. Nors *III-V* grupės puslaidininkiai labiau tinka projektuojant vatų eilės išėjimo galios belaidžio ryšio GS, tuo tarpu įvairialyčio (angl. heterogenous) tinklo struktūra numato šimtų milivatų eilės išėjimo signalų galias. Todėl atsiveria galimybės panaudoti KMOP puslaidininkių gamybos technologijas. Dėl paminėtų priežasčių būtina ieškoti belaidžio ryšio KMOP GS architektūrų sprendimų, kurie galėtų užtikrinti 5G

standarto reglamentuojamas siunčiamų signalų galias, prie sumažintų veikimo srovių (angl. quiescent current) bei plačiame stiprinamo signalo galių ruože.

5G tinkluose numatoma naudoti ne tik decimetrinių, bet ir centimetrinių bei milimetrinių bangų ruožai. 3GPP standartas (European Standards Organization ETSI, 2018) reglamentuoja tik dvi 5G juostų grupes, pavadintas FR1 (iki 6 GHz) ir FR2 (virš 24 GHz), tačiau neįvertina nelicencijuotų dažnių Europoje (5,9–6,4 GHz) ir JAV (5,9–7,1 GHz). Visas 1–7,1 GHz dažnių ruožas, kuris įtraukia liceencijuotų ir nelicencijuotų dažnių juostas, pavadintas vidutinių dažnių 5G juosta (Qualcomm Technologies Inc., 2017). Toks dažnių juostų apjungimas yra galimas dėl to, kad minėti tiek licencijuoti, tiek nelicencijuoti dažnių ruožai skirti bendros paskrities ir lokaliam padidintos spartos ryšiui, ir būtent šiuose dažniuose veikiančiai įrangai ir skiriamas didžiausias prioritetas. Taip pat minimos žemų (iki 1 GHz) ir aukštų (virš 24 GHz) dažnių juostos. Tuo tarpu aukštų dažnių ruožas yra numatytas itin sparčiam lokaliam duomenų perdavimui. Prie skirtingų galios lygių efektyviai veikiantys GS taip pat turi būti pritaikomi visose numatomose 5G dažnių juostose be linearizavimo galimybių apribojamų.

Atliekant GS (tai taip pat gali būti ir kitų aukštadažnių grandynų) eksperimentinius tyrimus, susiduriama ir su suderinimo grandynų, kurie suderina šaltinį su apkrova, projektavimo problemomis. Suderinimo grandinės dažniausiai įgyvendinamos lusto išorėje, nes didelis kiekis integruotų induktyvumo ričių sąlygotų didelę lusto gamybos kainą. Todėl impedansų suderinimo grandinės projektuojamos lusto išorėje iš diskretinių sutelktųjų parametrų komponentų. Tačiau šie komponentai turi parazitinius parametrus, įtakojančius minimalaus S_{11} parametro gavimą prie ieškomo dažnio. Todėl, neįvertinus parazitinių suderinimo komponentų parametrų, tam prireikia daug skaičiavimų ir matavimų iteracijų, sąlygojančių didelę projektavimo trukmę ir suderinimo grandynų bei eksperimentinių tyrimų kainą. Kadangi iki šiol nėra pasiūlytas metodas, kuris įvertina šių komponantų parazitinius parametrus, būtina ieškoti metodų ir kurti programinius įrankius, leidžiančius įvertinti šių suderinimo grandinių, skirtų naujos kartos belaidžio ryšio GS, komponentų parazitinius parametrus.

Įvertinant tai, kad naujos kartos 5G belaidžio ryšio įranga bus įvairialytė bei mobili, numatomos daugiakanalio ryšio galimybės ir ženkliai išaugęs šios įrangos tankis, suformuluojama pagrindinė disertacijoje sprendžiama problema – nešiojamų vidutinių dažnių 5G belaidžio ryšio įrenginių KMOP galios stiprintuvo su suderinimo grandynais veikimo efektyvumo didinimas. Problemai išspręsti iškeliama ir įrodoma darbinė hipotezė: Doherty architektūros galios stiprintuvas su suderinimo grandynais, suprojektuotas taikant giliai submikronines KMOP technologijas, gali užtikrinti efektyvumo padidėjimą plačiame įėjimo signalų galių diapazone ir yra tinkamas kuriant naujos kartos 5G ryšio sistemas.

Darbo aktualumas

Šiuolaikinio belaidžio ryšio tinklo struktūra sparčiai vystosi ir įsigalėjus 4G standartui, pradedamas plėtoti naujos kartos 5G belaidžio ryšio standartas bei ateities tinklo modeliai. Lyginant su ketvirtos kartos 4G ryšio standartu, 5G tinkle planuojama pasiekti duomenų apsikeitimo spartas nuo 100 Mbit/s iki 1 Gbit/s, užtikrinti iki 1 milijono viename kvadratiniame kilometre ryšio klientų tankį, milisekundžių eilės sujungimo

delsos laikus, iki 150 MHz veikimo juostos pločius ir iki 500 km/h galimą klientų judėjimo greitį (The European Conference of Postal and Telecommunications Administrations CEPT, 2018). Naujos kartos belaidžio ryšio tinklo struktūra, pereidama nuo didelės galios siųstuvų-imtuvų bokštų link įvairialyčio tinklo, sudaryto iš daugelio mažos galios siųstuvų-imtuvų, gali apjungti daiktų (angl. Internet of Things, IoT) ir transporto priemonių internetą (angl. Internet of Vehicles, IoV) į vieną bendrą daugialypį tinklą (angl. Internet of Everything, IoE). Todėl naujos kartos 5G belaidžio ryšio technologijos taps svarbiausia 4-osios pramonės revoliucijos (angl. Industry 4.0) dalimi. Įvairialyčių 5G tinklų struktūroje taip pat numatytos ryšio galimybės su mažos galios nešiojamais jutikliais, maitinamais iš nešiojamų energijos šaltinių, ir tokios technologijos reikalauja efektyvių siųstuvų-imtuvų. Kadangi GS apsprendžia visos siųstuvo grandies efektyvumą, būtini tyrimai mažos galios KMOP GS architektūrų ir jiems skirtų suderinimo grandynų srityje (Rao & Prasad, 2018). Dėl to, kad paskelbtos tendencijos mažinti siųstuvų-imtuvų galią, vis daugiau mokslinių tyrimų orientuojama į mažų ir vidutinių galių belaidžio ryšio elementų ir sistemų kūrimą, taikant jau ištobulintas submikronines KMOP technologijas. Šiuo metu sukurta daugybė klasikinės bei pažangios GS architektūrų ir jų modfikacijų, tačiau nėra aišku kurio tipo architektūra yra tinkama naudoti naujos kartos belaidžio ryšio įrangoje, atitinkančioje 5G įvairialyčio tinklo keliamus reikalavimus. Submikroniniai KMOP gamybos procesai pasirenkami tuomet kai reikalingas didelės integracijos ir funkcionalumo derinys. Todėl, pasirinkus submikronines KMOP gamybos technologijas, skaitmeniniai valdymo blokai gali būti integruojami kartu su GS ir kitais aukštadažniais grandynais viename luste (Zampardi, 2010). Ši tendencija taip pat pastebima analizuojant rinkoje pirmaujančių siųstuvų-imtuvų gamintojų integrinius grandynus (Analog Devices, 2019; Lime Microsystems, 2019; Texas Instruments, 2019).

Lietuvoje moksliniai tyrimai susiję su belaidžio ryšio grandynais nėra plačiai paplitę. Šia tematika tyrimo rezultatus publikuoja VGTU mokslininkai M. Jurgo (Jurgo et al., 2019), V. Mačaitis (Mačaitis et al., 2019), K. Kiela (Kiela, et al., 2016), J. Charlamov (Charlamov et al., 2010), bei VU mokslininkas P. Sakalas (Sakalas et al., 2008). Taip pat tyrimus belaidžio ryšio bei sparčiųjų integrinių grandynų srityje atlieka Vilniuje ir Kaune įsikūrusios uždarosios akcinės bendrovės „Lime Microsystems“ ir „Si Femto“.

Apibendrinant galima teigti, kad naujos kartos 5G belaidžių tinklų aukštadažnių galios stiprintuvai ir jų impedansų suderinimo grandynai nėra pakankamai ištirti ir aprašyti, darbe vykdomi tyrimai yra aktualūs, o gauti rezultatai bei tolimesni tyrimai paspartins naujos kartos 5G belaidžio ryšio vystymąsi.

Tyrimo objektas

Darbo tyrimų objektas – vidutinių dažnių 5G belaidžio ryšio galios stiprintuvų architektūros su joms skirtais suderinimo grandynais.

Darbo tikslas

Disertacijos tikslas yra ištirti ir pasiūlyti galios stiprintuvų architektūras su originaliais jų suderinimo grandynų apskaičiavimo metodais, tinkamas vidutinių dažnių 5G belaidžio ryšio sistemų kūrimui.

Darbo uždaviniai

Darbo tikslui pasiekti buvo sprendžiami šie uždaviniai:

1. Atlikti išsamius įvairių belaidžio ryšio galios stiprintuvų architektūrų tyrimus, pateikiant kokybinės ir kiekybinės analizės rezultatus.
2. Sukurti ir eksperimentiškai ištirti skirtingų architektūrų belaidžio ryšio galios stiprintuvus, išskiriant tinkamiausią vidutinių dažnių 5G belaidžio ryšio sistemoms kurti.
3. Išnagrinėti impedansų suderinimo grandynų apskaičiavimo metodus bei pasiūlyti originalų algoritmą ir matematinį modelį sutelktųjų parametrų komponentų parazitiniams parametrams apskaičiuoti ir juos įvertinti belaidžio ryšio stiprintuvų projektavime.

Tyrimų metodika

Belaidžio ryšio galios stiprintuvų architektūroms bei impedansų suderinimo grandynams tirti taikyti analitiniai, matematiniai, kompiuterinio modeliavimo ir eksperimentiniai tyrimo metodai. Analitiniai metodai buvo taikomi apibendrinant įvairias belaidžio ryšio galios stiprintuvų architektūras ir impedanso suderinimo grandynų projektavimo metodus. Įvairių belaidžio ryšio galios stiprintuvų architektūrų ir impedansų suderinimo grandynų tyrimų metu buvo taikomi matematiniai, kompiuteriniai modeliavimo ir eksperimentiniai metodai. Projektuojant klasikinius, bėgančiosios bangos ir Doherty architektūrų belaidžio ryšio galios stiprintuvus buvo panaudotos *TSMC* 0,18 µm ir *IBM (GlobalFoundries)* 0,13 µm giliai submikroninės KMOP gamybos procesų technologinės bibliotekos. Suprojektuoti belaidžio ryšio galios stiprintuvai buvo modeliuojami taikant profesionalų integrinių grandynų projektavimo *Cadence Virtuoso* programų paketą. Pasiūlytas impedansų suderinimo grandynų sintezavimo įskiepis *IMNS Toolbox* buvo sukurtas taikant *OCEAN* ir *SKILL* programavimo kalbas ir įdiegtas *Cadence Virtuso* aplinkoje. Spausdintinių plokščių, skirtų suprojektuotų stiprintuvų ir suderinimo grandynų testavimui ir tyrimams, projektavimui panaudota *Altium Designer* programinė įranga. Belaidžio ryšio galios stiprintuvai ir suderinimo grandynai buvo tiriami 0,1–7,1 GHz dažnių ruože, priklausančiame vidutinių dažnių 5G belaidžio ryšio dažnių juostai.

Mokslinis naujumas

Rengiant disertaciją buvo gauti šie elektros ir elektronikos inžinerijos mokslui reikšmingi rezultatai:

1. Pasiūlytas kokybinis ir kiekybinis naujausių belaidžio ryšio galios stiprintuvų architektūrų vertinimas, išskiriant šių architektūrų privalumus ir trūkumus, giliai

submikroninių (0,35–0,11 μm) KMOP technologijų tranzistorių matmenų mažinimo įtaką stiprintuvo parametrams, bei pritaikomumą naujos kartos tiek žemų, tiek vidutinių, tiek aukštų dažnių 5G belaidžio ryšio siųstuvams bei siųstuvams-imtuvams kurti.

2. Pasiūlyta klasikinio Doherty galios stiprintuvo architektūros modifikacija, leidžianti supaprastinti išėjimo impedansų inverterį, taip 12 % sumažinant užimamą plotą luste, taikant (0,35–0,11 μm) giliai submikronines KMOP technologijas, išlaikant efektyvumą artimą įsisotinimo efektyvumui 3 dB atgalinės galios ruože.
3. Pasiūlytas naujas sutelktųjų parametrų impedansų suderinimo grandynų sintezės algoritmas ir matematinis modelis, leidžiantys įvertinti komponentų parazitinius parametrus, pakuotės dydį, dielektrinės medžiagos savybes bei veikimo dažnių diapazoną.

Darbo rezultatų praktinė reikšmė

Pasiūlytas kokybinio ir kiekybinio vertinimo metodika gali būti naudojama, įvertinant skirtingų gamybos technologijų galios stiprintuvų architektūras, ir kuriant naujos kartos tiek žemų, tiek vidutinių, tiek aukštų dažnių juostų 5G belaidžio ryšio sistemas. Disertacijoje tirtos architektūros buvo suprojektuotos ir pagamintos taikant *TSMC* 0,18 μm ir *IBM (GlobalFoundries)* 0,13 μm giliai submikronines KMOP gamybos technologijas. Pasiūlyta klasikinės Doherty architektūros modifikacija gali būti panaudojama naujos kartos vidutinių dažnių 5G siųstuvuose bei siųstuvų-imtuvų projektavime ir tyrimuose. Įgyvendinti impedansų suderinimo grandynų sintezės matematinis modelis ir algoritmas bei jų pagrindu sukurta programinė įranga, leidžia sumažinti galios stiprintuvams skirtų grandynų projektavimo trukmę ir gamybos kaštus. Profesionaliame integrinių grandynų projektavimo *Cadence Virtuoso* programų pakete įdiegtas *IMNS Toolbox* įskiepis gali būti pritaikomas sprendžiant aukštadažnių grandynų inžinerinius uždavinius ir vykdant mokslinius tyrimus.

Disertacijos tyrimų rezultatai buvo panaudoti vykdant:

- Ūkio subjekto užsakomąjį projektą „Išmaniosios aktyvinės kortelės projektavimas“. Užsakovas: UAB „Vildoranas“, UAB „STAV“. 2014–2015. Sutarties Nr. VP2-1.3-ŪM-05-K-03-825, Nr. 11796.
- Ūkio subjekto užsakomąjį projektą „Aukštadažnių integrinių grandynų išmaniesiems daugiastandarčiams siųstuvams-imtuvams projektavimas ir tyrimas“. Užsakovas: UAB „Lime Microsystems“. 2014–2015. Sutarties Nr. 10124.
- Ūkio subjekto užsakomąjį projektą „Testinių spausdintinių plokščių kūrimas ir projektavimas daugiastandarčiams siųstuvams-imtuvams“. Užsakovas: UAB „Lime Microsystems“. 2016–2017. Sutarties Nr. 15222.
- Lietuvos mokslo tarybos (LMT) finansuotą projektą „4G ir ateities 5G belaidžio ryšio aukštadažnių galios stiprintuvų architektūrų tyrimas“. 2017–2018. Paraiškos Nr. 09.3.3.-LMT-K-712-03-0007.
- Ūkio subjekto užsakomąjį projektą „Šiuolaikinio ypač mažų matmenų, didelės duomenų perdavimo spartos šarvuotų durų užrakto stebėjimo sistemos maketo kūrimas“. Užsakovas: UAB „ICUS LT“. 2017–2018. Sutarties Nr. 17582.

− Lietuvos mokslo tarybos (LMT) aukšto lygio tyrėjų grupių vykdomų mokslinių tyrimų projektą „Daiktų interneto karkaso modelio ir priemonių intelektualioms transporto sistemoms kūrimas ir tyrimas“. 2017–2019. Paraiškos Nr. 01.2.2-LMT-K-718-01-0054.

Ginamieji teiginiai

1. Klasikinės tiesinės ir bėgančiosios bangos architektūros belaidžio ryšio galios stiprintuvai, kurie suprojektuoti taikant *IBM (GlobalFoundries)* 0,13 μm giliai submikroninę KMOP gamybos technologiją, yra netinkami vidutinių dažnių 5G belaidžiams siųstuvams ir siųstuvams-imtuvams kurti, dėl abiejų architektūrų mažesnio nei 25 % efektyvumo veikiant prie skirtingų įėjimo signalo galių ir klasikinio stiprintuvo veikimo dažnio diapazono apribojimų (iki 400 MHz).
2. Doherty architektūros galios stiprintuvai, suprojektuoti taikant *TSMC* 0,18 μm giliai submikroninę KMOP technologiją, gali užtikrinti efektyvumą tarp 25 % ir didžiausio teorinio 50 %, esant 3 dB atgalinei galiai ties 6,5 GHz centriniu dažniu.
3. Įvertinus paviršinio montažo sutelktųjų parametrų komponentų parazitinius parametrus, galima sumažinti suderinimo grandynų modeliavimų ir matavimų skaičių iki 1–3 iteracijų vidutinių 5G dažnių juostoje.
4. Siekiant suderinti šaltinio ir apkrovos impedansus bei naudojant sutelktųjų parametrų kondensatorius ir induktyvumo rites, tik pats jautriausias talpos (arba induktyvumo) vertės pokyčiams komponentas turi turėti mažiausią neapibrėžtumą (iki 5 %), o visi kiti komponentai gali turėti ir didesnį IEC/EN 60062 standarto reglamentuojamą vertės neapibrėžtumą.

Darbo rezultatų aprobavimas

Disertacijos tema paskelbtos trys publikacijos (Vasjanov & Barzdenas 2016; Vasjanov & Barzdenas 2018, Sep.; Vasjanov & Barzdenas 2018, Oct.) moksliniuose žurnaluose, referuojamuose *Clarivate Analytics Web of Science* duomenų bazėje, ir turinčiuose citavimo rodiklius, bei dvi publikacijos – konferencijų straipsnių rinkiniuose, iš kurių viena (Vasjanov & Barzdenas 2017) priskiriama *Clarivate Analytics Web of Science* duomenų bazės *Conference Proceedings* leidiniams, o antroji (Vasjanov & Barzdenas 2018, May) nereferuojamoje tarptautinės užsienio konferencijos „*CDNLive EMEA 2018: Cadence user conference*“ medžiagoje. Taip pat disertacijos vykdymo metu buvo paskelbtos dvi publikacijos nesusijusios su disertacijos tema, tačiau priskirtinos Elektros ir elektronikos mokslo krypčiai. Abu šie straipsniai publikuoti moksliniuose žurnaluose, referuojamuose *Clarivate Analytics Web of Science* duomenų bazėje ir turinčiuose citavimo rodiklius.

Disertacijoje atliktų tyrimų rezultatai buvo paskelbti devyniose mokslinėse konferencijose Lietuvoje ir užsienyje:

− Tarptautinėje mokslinėje konferencijoje „*CDNLive EMEA 2018: Cadence user conference*“, vykusioje Miunchene, Vokietijoje, 2018 m. gegužės 7–9 d. Šioje konferencijoje skaitytas kviestinis pranešimas.

- 2-ojoje tarptautinėje konferencijoje „*Electrical, Electronic and Information Sciences 2018 (eStream 2018)*“ vykusioje Vilniuje, 2018 m. balandžio 26 d.
- 21-ojoje Lietuvos jaunųjų mokslininkų konferencijoje „*Mokslas – Lietuvos ateitis. Elektronika ir elektrotechnika*“, vykusioje Vilniuje, 2018 m. kovo 16 d.
- 18-tame Lietuvos ir Baltarusijos IEEE skyrių seminare „*Advanced Microwave Devices and Systems*“, vykusiame Vilniuje, 2017 m. gruodžio 8–9 d.
- Ročesterio universiteto organizuotame seminare, vykusiame Ročesteryje, JAV, 2017 m. gegužės 9 d.
- 1-ojoje tarptautinėje konferencijoje „*Electrical, Electronic and Information Sciences 2017 (eStream 2017)*“ vykusioje Vilniuje, 2017 m. balandžio 27 d.
- Respublikinėje elektros, elektronikos ir informatikos mokslų konferencijoje „*Electrical, Electronic and Information Sciences 2016 (eStream 2016)*“, vykusioje Vilniuje, 2016 m. balandžio 19 d.
- 19-ojoje Lietuvos jaunųjų mokslininkų konferencijoje „*Mokslas – Lietuvos ateitis. Elektronika ir elektrotechnika*“, vykusioje Vilniuje, 2016 m. kovo 18 d.
- 16-tame Lietuvos ir Baltarusijos IEEE skyrių seminare „*Advanced Microwave Devices and Systems*“, vykusiame Vilniuje, 2015 m. gruodžio 4 d.

Disertacijos struktūra

Darbą sudaro įvadas, trys skyriai, išvados, literatūros sąrašas ir autoriaus publikacijų disertacijos tema sąrašas. Taip pat yra trys priedai. Darbo apimtis yra 151 puslapiai, neskaitant priedų, tekste panaudotos 70 numeruotų formulių, 59 paveikslai ir 21 lentelės. Rašant disertaciją buvo panaudoti 191 literatūros šaltiniai.

Padėka

Disertacijos autorius norėtų išreikšti savo nuoširdžią padėką mokslinio darbo vadovui, VGTU Kompiuterijos ir ryšių technologijų katedros docentui doc. dr. Vaidotui Barzdėnui už kantrybę, patarimus ir vertingas mokslines konsultacijas doktorantūros studijų metu.

Autorius taip pat norėtų padėkoti Aleksandrui Mamajevui už jo patarimus ir paraginimus tęsti mokslą doktorantūroje ir galimybę mokslus suderinti su darbą privačiame sektoriuje.

Dėkoju dr. Jonui Liobe už vertingas pastabas, rašant su disertacijos tema susijusias publikacijas. Dėkoju disertacijos ekspertams prof. habil. dr. Romualdui Navickui ir prof. dr. Šarūnui Paulikui bei dr. Karoliui Kielai bei komisijos recenzentams prof. dr. Algirdui Baškiui ir doc. dr. Vitalij Novickij už vertingas pastabas tobulinant disertacijos turinį. Taip pat norėčiau padėkoti visiems kolegoms iš VGTU Elektronikos fakulteto Kompiuterijos ir ryšių technologijų katedros už patarimus doktorantūros studijų metu.

Ačiū Lietuvos mokslo tarybai už suteiktą paramą, vystant mikro- ir nanoelektronikos mokslą Lietuvoje ir už suteiktas doktorantų paramos stipendijas Nr. DOK-17065, Nr. P-DAP-18-152 ir Nr. P-DAP-19-149.

Autorius taip pat labai dėkingas savo šeimai: tėvams Tamarai ir Vladimirui, močiutei Ninai ir sesutei Janai už jų paramą visų studijų metu.

1. Šiuolaikinių belaidžio ryšio galios stiprintuvų architektūrų apžvalga

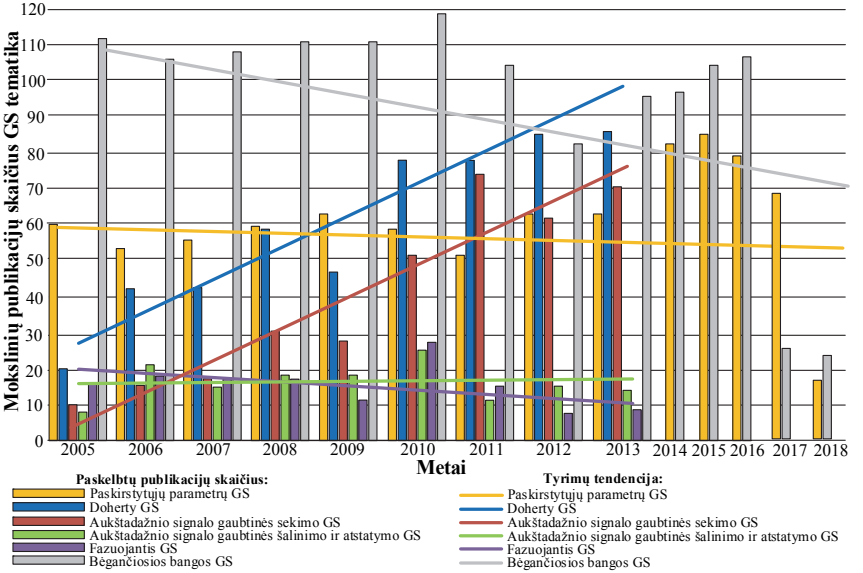
Šiuolaikinės belaidžio ryšio sistemos sudarytos iš daugelio prieigos mazgų, apimančių skirtingos išėjimo galios įrangą ir naudotojų skaičių. Pastaraisiais metais pastebima perėjimo, nuo tradicinės tinklo struktūros su pavieniais aukštos galios prieigos taškais (ryšio bokštais) prie įvairialytės architektūros, tendencija. Įvairialyčio tinklo elementai skirstomi pagal jų išėjimo galią į makro-, mikro-, piko-, femto-celes ir kt. Lyginant makro- ir femto-celes tarpusavyje, skiriasi tik išėjimo galia, o visa architektūra ir panaudojami blokai dažniausiai išlieka tokie patys. Makro-celės yra stacionarios bazinės stotys, kurios apdoroja aukštagalius (iki šimtų vatų) signalus ir kuriems dažniausiai reikalingi *III-V* grupės puslaidininkių pagrindu sukurti galios stiprintuvai.

Nepaisant to, kad belaidžio ryšio siųstuvai ir siųstuvai-imtuvai gali būti projektuojami taikant vien tik *III-V* grupės puslaidininkių technologijas, šių technologijų integracijos laipsnis netinka didelio tankio skaitmeniniams grandynams kurti dėl ypač didelio gamybos kainos ir integracijos laipsnio santykio. Taip pat šios grupės puslaidininkių technologijos nėra tinkamos nešiojamoms, mažų galių celėms. Tuo tarpu šių paminėtų trūkumų neturi KMOP technologijos, užtikrinančios tiek didelį integravimo laipsnį, tiek mažas vartojamąsias galias bei pritaikomumą mažos galios signalų siuntimui. Juolab, kad KMOP technologijos yra ištobulintos bei masteliuojamos, o jų pagrindu sukurtų lustų gamybos kainos kelis kartus mažesnės negu tų, kurie sukurti naudojant *III-V* grupės puslaidininkius. KMOP tranzistorių didžiausia leistina įtampa (angl. breakdown voltage) ženkliai mažesnė už didžiausią leistiną *III-V* grupės tranzistorių įtampą, tačiau šios technologijos puikai tinka siekiant suderinti skaitmeninius ir analoginius blokus viename mažos galios integriniame grandyne.

Publikacijos (Cheng et al., 2015) autoriai atliko tyrimą, kurio tikslas buvo nustatyti belaidžio ryšio galios stiprintuvų tyrimo krypčių tendencijas per pastaruosius metus. Buvo išanalizuota daugiau negu 1000 publikacijų ir šio tyrimo rezultatų suvestinė pateikta S1.1 paveiksle. Šio straipsnio autoriai išskyrė keturias plačiausiai naudojamas ir labiausiai ištobulintas belaidžio ryšio galios stiprintuvų architektūras – *Doherty*, *aukštadažnio signalo gaubtinės šalinimo ir atkūrimo* (angl. envelope elimination and restauration), *aukštadažnio signalo gaubtinės sekimo* (angl. envelope tracking) ir *fazuojančius stiprintuvus* (angl. outphasing). Šioje disertacijoje šie tyrimo rezultatai buvo papildyti, apibendrinant *paskirstytųjų parametrų* (angl. distributed amplifier) ir *bėgančiosios bangos stiprintuvų* (angl. traveling wave amplifier) mokslinių tyrimų rezultatus. Apibendrinant S1.1 paveiskle pateiktus rezultatus galima pažymėti, kad bėgančiosios bangos ir paskirstytųjų parametrų bei Doherty galios stiprintuvų architektūros buvo labiausiai tiriamos per pastaruosius 10 metų.

Pasiūlytas kokybinis ir kiekybinis vertinimas gali būti naudojamas, įvertinant skirtingų gamybos technologijų galios stiprintuvų architektūras, ir kuriant naujos kartos tiek žemų, tiek vidutinių, tiek aukštų dažnių juostų 5G belaidžio ryšio sistemas. Šis vertinimas buvo pritaikytas, analizuojant pažangiąsias GS architektūras 0,35 μm – 28 nm KMOP technologijose. Remiantis atlikta išsamia literatūros apžvalga, klasikinės tiesinės belaidžio ryšio galios stiprintuvų architektūros pasižymi dideliu tiesiškumu, tačiau prastu efektyvumu (5–20 %).

Literatūroje minimos tokios pažangios galios stiprintuvų architektūros, kaip žemadažnio signalo gaubtinės sekimo, fazuojantis, Doherty ir bėgančiosios bangos galios stiprintuvai. Didžiausias žemadažnio signalo gaubtinės sekimo galios stiprintuvo veikimo dažnių diapazonas aplink nešlį yra 40 MHz. Šios architektūros galios stiprintuvo efektyvumas yra 17–48 % ribose, tačiau, dėl jos sudėtingumo, į siunčiamą signalą patenka papildomų triukšmų.



S1.1 pav. Belaidžio ryšio galios stiprintuvų tyrimų tendencijos

Fazuojančio GS efektyvumas yra 20–60 % ribose, o didžiausias veikimo dažnių ruožas neviršija 40 MHz. Doherty architektūros galios stiprintuvas užtikrina iki 500 MHz veikimo dažnių ruožą aplink nešlį, 20–5 % efektyvumą bei pasižymi pastoviu efektyvumo lygiu tam tikrame įėjimo signalo lygių diapazone. Bėgančiosios bangos GS pasižymi veikimo dažnių juosta iki 80 GHz ir yra vienintelė KMOP technologijos galios stiprintuvo architektūra, kuri prilygsta *III-V* grupės stiprintuvams. Taip pat pastebėta, kad KMOP tranzistorių mažinimas ne visuomet užtikrina GS parametrų pagerėjimą bei stiprintuvai, kurie sukurti 0,13–0,18 µm KMOP pagrindu užtikrina didžiausią stiprinimo koeficiento, efektyvumo ir veikimo dažnių juostos santykį su lusto kaina (analizuoti 0,35 µm – 28 nm KMOP technologijų stiprintuvai).

5G yra sekantis belaidžio ryšio tinklo evoliucijos etapas, įvedantis esamai telekomunikacijų infrastruktūrai tiek naujų patobulinimų, tiek sukuriantis naujų iššūkių. Šios belaidžio ryšio technologijos skirtos užtikrinti dideles duomenų spartas ir ypač mažos delsos duomenų apsikeitimą tarp įvairių įtaisų, taip sukuriant visapusišką duomenų apdorojimo ekosistemą, susiejančią tarpusavyje visus ryšio įrenginius (Sarfaraz & Hammainen, 2017).

Tokios organizacijos, kaip Europos pašto ir telekomunikacijų administracijų konferencija (The European Conference of Postal and Telecommunications Administrations CEPT, 2018) ir JAV Federalinė ryšių komisija (Federal Communications

Commission FCC, 2018), nustato 5G ryšio dažnių juostas Europoje ir JAV. 3GPP standartas (European Standards Organization ETSI, 2018) licencijuotas dažnių juostas dalina į dvi grupes, kurios pavadintos FR1 (iki 6 GHz) ir FR2 (iki 24 GHz). Minėtas standartas neįtraukia nelicencijuotas dažnių juostas Europoje (5.9–6.4 GHz) ir JAV (5.9–7.1 GHz). Tiek licencijuotos, tiek minėtos nelicencijuotos juostos yra įtrauktos į FR1 grupę, suteikus pavadinimą vidutinių dažnių 5G juosta (Qualcomm Technologies Inc., 2017). Taip pat minimos ir žemų (iki 1 GHz) ir aukštų (virš 24 GHz) dažnių juostos. Numatoma žemų dažnių juostą (iki 1 GHz) naudoti lokaliam ryšiui užtikrinti. Vidutinių dažnių juosta (iki 7 GHz) numatyta didelės spartos ryšio kanalui užtikrinti, Daiktų Internetui (angl. Internet of Things) bei automobilio ir kitos eismo įrangos (angl. vehicle-to-everything) duomenų apsikeitimui. O tuo tarpu milimetrinių bangų (auktų dažnių) ruožas bus skirtas itin didelės spartos lokaliems belaidžio ryšio taškams (angl. wireless hotspots) sukurti (GSMA Spectrum, 2016). Minimi ir kiti 5G ryšio specifikacijų parametrai: didžiausia nešiojamų įrenginių spinduliuojama galia iki 24 dBm (251 mW), duomenų apsikeitimo spartos nuo 100 Mbit/s iki 1 Gbit/s, ryšio klientų tankis iki 1 milijono viename kvadratiniame kilometre, milisekundžių eilės sujungimo delsos laikai ir iki 500 km/h galimas klientų judėjimo greitis (The European Conference of Postal and Telecommunications Administrations CEPT, 2018).

Remiantis atlikta išsamia literatūros apžvalga, klasikinių tiesinių belaidžio ryšio GS architektūra pasižymi dideliu tiesiškumu, tačiau prastu efektyvumu (5–20 %). Literatūroje minimos tokios pažangios galios stiprintuvų architektūros, kaip žemadažnio signalo gaubtinės sekimo, fazuojantis, Doherty ir bėgančiosios bangos GS. Žemadažnio signalo gaubtinės sekimo stiprintuvo architektūra pasižymi sudėtinga struktūra, papildomais triukšmais siuntimo grandinėje ir žemadažnio signalo juostos pločio apribojimais. Bėgančiosios bangos stiprintuvo platus veikimo dažnių ruožas pasiekiamas dėka suformuojamos *LC* mikrojuostelinės linijos, tačiau dėl didelio integrinių induktyvumo ričių skaičiaus išauga ir užimamas lusto plotas. Tuo tarpu, fazuojančio stiprintuvo praktinis efektyvumas yra žymiai prastesnis negu teorinis veikimo efektyvumas. Taip pat pastebėta, kad KMOP tranzistorių mažinimas ne visuomet užtikrina GS parametrų pagerėjimą bei stiprintuvai, kurie sukurti 0,13–0,18 μm KMOP pagrindu užtikrina didžiausią stiprinimo koeficiento, efektyvumo ir veikimo dažnių juostos santykį su lusto kaina (analizuoti 0,35 μm – 28 nm KMOP technologijų GS).

Atlikus analitinę pažangiųjų GS architektūrų apžvalgą, gilesniems eksperimentiniams ir praktiniams tyrimams pasirinktos dvi iš keturių mokslinėse publikacijose skelbiamų architektūrų – Doherty ir bėgančiosios bangos GS. Fazuojančio ir žemadažnio signalo gaubtinės sekimo GS architektūros yra netinkamos 5G įtaisams kurti dėl sudėtingos struktūros, tarpinio dažnio juostos (angl. intermediate frequency, IF) bei linearizavimo apribojimų ir papildomų triukšmų siuntimo grandinėje. Taip pat nuspręsta atlikti tyrimus su įvairiomis klasikinėmis GS konfigūracijomis giliai submikroninėse KMOP technologijose, kadangi klasikinis GS yra pagrindas, kuriant tiek Doherty tiek bėgančiosios bangos GS.

2. Impedansų suderinimo grandynų tyrimas, projektavimas ir sintezė

Neatsiejama bet kokio aukštadažnio belaidžio ryšio GS dalis yra impedansų suderinimo grandynai. Suderinimo grandinės dažnai suformuojamas lusto išorėje dėl didelio integrinių induktyvumo ričių užimamo ploto, taip sudarant galimybes atlikti suderinimo atsako S_{11} korekcijas. Projektuojant suderinimo grandines su sutelktais parametrais, susiduriama modeliuojamų ir matuojamų S_{11} atsakų neatitikimu dėl komponentų parazitinių parametrų. Tokiu būdu reikalingos kelios iteracijos, siekiant suderinti galios stiprintuvą su apkrova taikant paskirstytųjų parametrų elementus.

Disertacijoje šis tikslas kilo dėl problemų, su kuriomis buvo susidurta pradinėje suprojektuotų galios stiprintuvų integrinių grandynų eksperimentinių tyrimų stadijoje. Apskaičiuojant suderinimo grandynus pagal klasikinę impedansų suderinimo teoriją pastebėta, kad suderinimo charakteristikos S_{11} minimumas neatitinka apskaičiuotą dažnį kai naudojami sutelktųjų parametrų komponentai. Reikėjo daug modeliavimo ir matavimo iteracijų tam, kad apkrovą tiksliai suderinti su šaltiniu reikiamam dažniui. Todėl buvo nuspręsta atlikti tyrimus, pagerinančius sutelktųjų parametrų komponentų suderinimo grandynų apskaičiavimo metodiką.

Mokslinėje literatūroje publikuoti įvairūs impedansų suderinimo grandynų jungimai ir konfigūracijos, tarp kurių yra fiksuotos bei valdomos paskirstytųjų ir sutelktųjų parametrų komponentų grandynai. Sutinkami ir mišrūs suderinimo grandynai, kuriuose panaudoti skirtingo tipo komponentai: puslaidininkiniai, mikro-elektromechaniniai (angl. MEMS) bei nano-elektromechaniniai (angl. NEMS) jungikliai. Taip pat pasiūlyti įvairūs suderinimo grandynų apskaičiavimo metodai, tačiau nei viename iš pateiktųjų nėra įvertinamos sutelktųjų parametrų komponentų parazitinės charakteristikos. Paskelbtame (Yuan & Suzuki, 2016) straipsnyje siūloma įskaičiuoti ekvivalentinę nuosekliąją komponentų varžą *ESR*, tačiau ji neturi įtakos nepageidaujamiems suderinimo charakteristikų S_{11} poslinkiams dažnių juostoje. Todėl atsižvelgus į tai, kad iki šiol mokslinėje literatūroje nebuvo publikuotas metodas, kuris skirtas padidinti apskaičiuotų ir išmatuotų suderinimo grandynų charakteristikų atitikimą, šioje disertacijoje pasiūlytas sutelktųjų parametrų impedansų suderinimo grandynų sintezės (ISGS) algoritmas, kuris pavaizduotas S2.1 paveiksle.

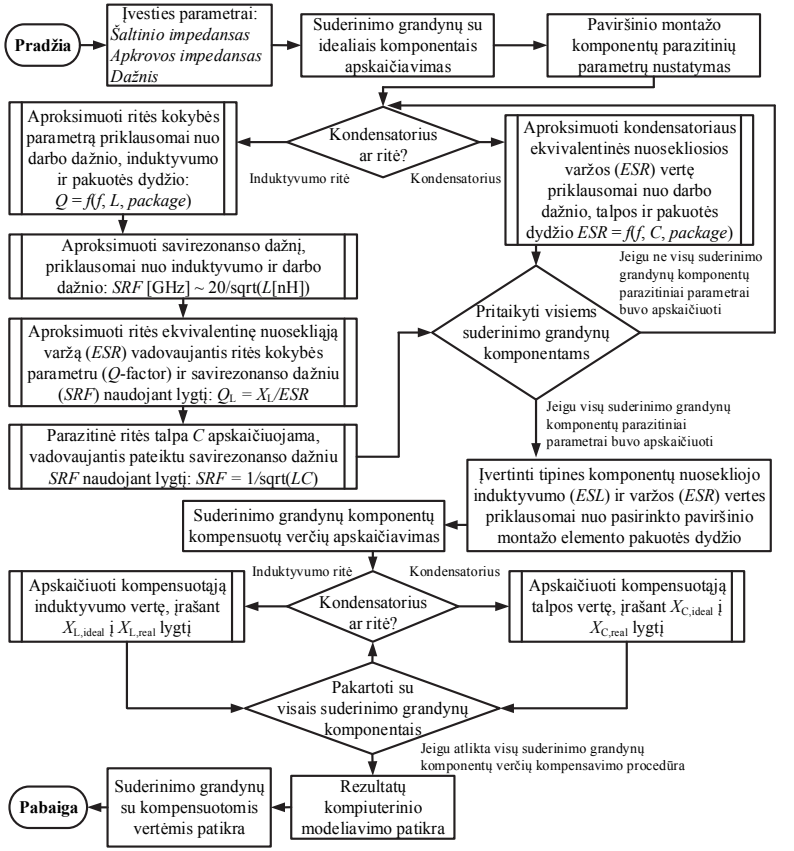
Šio algoritmo tikslas yra kompensuoti impedansų suderinimo grandynų komponentų nominalus, apskaičiuotus taikant klasikinę teoriją. Pasiūlytas algoritmas pagrįstas paviršinio montažo kondensatorių ir induktyvumo ričių parazitinių parametrų, tokių kaip ekvivalentinės nuosekliosios varžos *ESR*, induktyvumo *ESL* bei nuotėkio varžos R_d įtaka šių komponentų kokybei Q (angl. Q-factor) bei savirezonansiniam dažniui *SRF*.

Išvardinti parazitiniai parametrai to paties nominalo kondensatoriui ar ritei yra skirtingi, nes jie priklauso nuo paviršinio montažo komponento pakuotės dydžio bei veikimo dažnio. Taip pat šie parazitiniai parametrai įtakoja grandynų suderinimo kokybės S_{11} charakteristikų, gautų modeliavimo ir eksperimentinio matavimo metu, neatitikimą.

Neįvertinus šių parametrų, suderinimo charakteristika pasislenka į žemesnių dažnių ruožą atžvilgiu ieškomo centrinio dažnio. Tokiu būdu, siekiant apkrovą tiksliai suderinti su šaltiniu tam tikrame dažnių ruože, būtina įvertinti kiekvieno suderinimo grandyno komponento parazitinius parametrus, taip sumažinant skaičiavimų, modeliavimų ir

matavimų iteracijų skaičių. Naujai pasiūlytas impedansų suderinimo grandynų sintezės algoritmas ir matematinis modelis buvo įgyvendinti profesionaliame integrinių grandynų projektavimo *Cadence Virtuoso* programiniame pakete, *IMNS Toolbox* įskiepio pavidalu.

Pasiūlytas naujas ISGS algoritmas, matematinis modelis ir *IMNS Toolbox* įskiepis buvo patikrinti atlikus eksperimentinius tyrimus. Buvo apskaičiuoti $Z_S = 50\ \Omega$ šaltinio ir $10\ \Omega$ apkrovos suderinimo grandynai esant skirtingiems centriniams dažniams. Eksperimentinių matavimų metu buvo panaudotas *HP8753E* sukalibruotas vektorinis grandynų analizatorius.

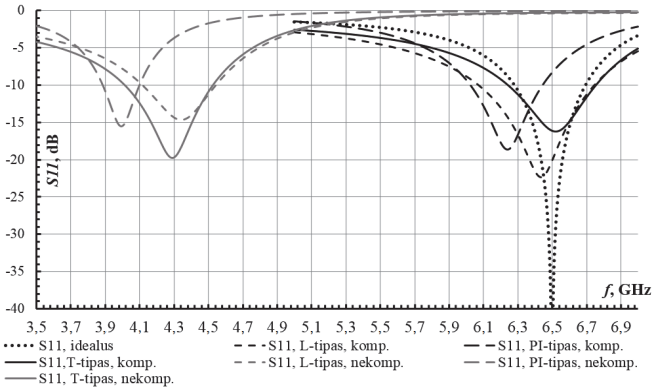


S2.1 pav. Pasiūlytas naujas ISGS algoritmas, įvertinantis komponentų parazitinius parametrus

Suderinimo grandynų su 10 % neapibrėžtimi 0402 paviršinio montažo komponentais modeliavimų ir matavimų rezultatai, esant 500 MHz, 1,5 GHz, 2,5 GHz ir 3 GHz centriniams dažniams. Eksperimentiškai ištirta, kad pasiūlytas naujas ISGS algoritmas leidžia sumažinti suderinimo charakteristikos nuokrypį iki 0,08 % (0,92 % pagerėjimas, lyginant su suderinimo grandynais kurios apskaičiuotos taikant klasikinę teoriją) esant 500 MHz centriniam dažniui, ir 2 % (2,16 % pagerėjimas, lyginant su suderinimo grandynais kurios apskaičiuotos taikant klasikinę teoriją) nuokrypį nuo 1500 MHz centrinio dažnio Prie

2,5 GHz ir 3 GHz nustatytas iki 8,1 % didžiausias nuokrypis nuo centrinio dažnio, kas atitinka 7 % pagerėjimą lyginant su klasikine teorija. Šis algoritmas sumažina projektuojamų suderinimo grandynų modeliavimo ir matavimo iteracijų skaičių iki 1 iteracijos 1 MHz – 1 GHz dažnių ruože ir iki 1–3 iteracijų, kai ruožas yra 1–3 GHz, o didžiausias nuokrypis nuo ieškomo centrinio dažnio sumažėjo iki 1–7 %, lyginant su klasikine teorija.

Atlikus šiuos tyrimus, prieita prie išvados, kad siekiant atlikti impedansų suderinimą naudojant mažiausią kiekį itin mažos neapibrėžties (iki 5 %) komponentų, būtina nustatyti suderinimo grandyno komponentą, kurio nominalo pokyčiai labiausiai paveikia suderinimo charakteristikos poslinkį dažnių ašyje. Šiam komponentui rekomenduojama naudoti bent 5 % nominalo neapibrėžtis. Tuo tarpu kitų suderinimo grandyno komponentų nominalai gali būti su bendros paskirties neapibrėžtimi remiantis IEC/EN 60062 standartu.



S2.2 pav. *L*-, *π*- ir *T*-tipo suderinimo grandynų,modeliavimo rezultatai vidutinių dažnių 5G juostoje esant 6,5 GHz centriniam dažniui

Pasiūlytas algoritmas taip pat buvo tirtas ir nelicencijuotos vidutinių dažnių 5G juostos ribose ties 6,5 GHz centriniu dažniu. Modeliavimo rezultatai pateikti S2.2 paveiksle. Ištyrus *L*-, *π*- ir *T*-tipo suderinimo grandynus su parazitiniais parametrais ties 6,5 GHz centriniu dažniu nustatyta, kad S_{11} charakteristikos nuokrypis sudaro iki 300 MHz (4,6 % nuo centrinio dažnio) kai panaudojamos kompensuotos (pagal pasiūlytą algoritmą) komponentų vertės. Jeigu komponentų vertės yra apskaičiuotos pagal klasikinę teoriją, tačiau į jų modelį įtraukiami ir parazitiniai parametrai, nuokrypis nuo centrinio dažnio sudaro iki 1,5 GHz (23 % nuo centrinio dažnio). Tokiu būdu, pasiūlytas ISGS algoritmas ir matematinis modelis, skirti suderinimo grandynų komponentų kompensuotoms vertėms nustatyti, yra taikytinas vidutinių dažnių 5G stiprintuvams kurti ir tirti.

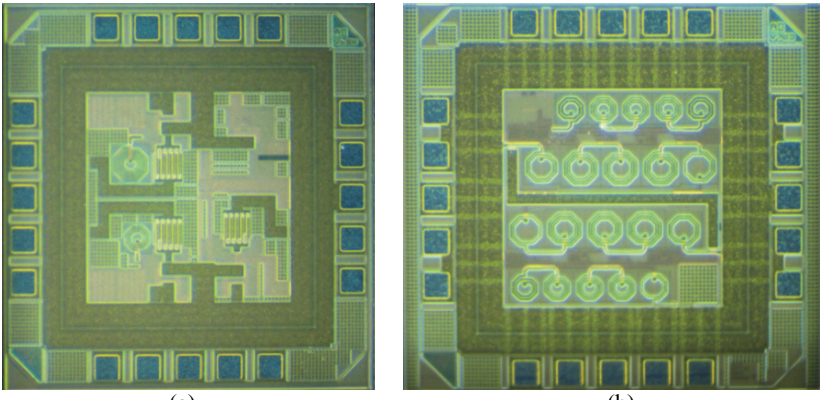
3. Belaidžio ryšio galios stiprintuvų tyrimas, projektavimas ir sintezė

Šioje disertacijoje buvo suprojektuoti, pagaminti ir ištirti du tiesinių belaidžio ryšio GS integriniai grandynai, taikant *IBM (GlobalFoundries)* 0,13 µm KMOP gamybos technologiją. Kiekvienas iš pagamintų integrinių grandynų turėjo kelias skirtingas GS konfigūracijas, siekiant palyginti tos pačios architektūros stiprintuvų konfigūracijas

tarpusavyje. Pirmasis pagamintas lustas (S3.1a pav.) sudarytas iš keturių atskirų, tiesinių klasikinės architektūros GS: vieno tranzistoriaus, kaskodinio su ir be grįžtamojo ryšio bei savaiminio užsimaitinimo galios stiprintuvų.

Teorinių ir eksperimentinių tyrimų metu, kuomet stiprintuvas suderintas 2,5 GHz centriniam dažniui (kuris yra LTE B41 ruožas, priklausantis vidutinių dažnių 5G juostai), nustatyta, kad klasikinės architektūros KMOP GS galima suderinti 200–400 MHz dažnių ruože. Vieno tranzistoriaus stiprintuvo konfigūracija užtikrina 35 % efektyvumą, tačiau tik apie 10 dB stiprinimą ir 200 MHz veikimo dažnio ruožą. Kaskodinės konfigūracijos GS su grįžtamuoju ryšiu užtikrina 300 MHz veikimo dažnių juostą, 14 dB stiprinimą ir išmatuotą 25 % efektyvumą. Kaskodinės konfigūracijos GS be grįžtamojo ryšio užtikrina 200 MHz veikimo dažnių juostą, 17 dB stiprinimą ir išmatuotą 25 % efektyvumą. Savaiminio užsimaitinimo GS užtikrina didžiausią 25 dB stiprinimą, plačiausią 400 MHz veikimo diapazoną, tačiau tik 17 % efektyvumą. Šie stiprintuvai taip pat buvo modeliuojami nelicencijuotos vidutinių dažnių 5G juostos ribose, esant 6,5 GHz centriniam dažniui. Tyrimai parodė, kad vieno tranzistoriaus, kaskodinio jungimo be ir su gįžtamuoju ryšiu bei savaiminio užsimaitinimo GS, esant įsisotinimui, užtikrina 16,2–27 % efektyvumą, o prie 3 dB atgalinės galios stiprintuvų veikimo efektyvumas sumažėja praktiškai dvigubai, iki 8,3–16,8 %.

Į antrąjį pagamintą lustą, kurio mikrofotografinė nuotrauka pavaizduota S3.1b paveiksle, buvo integruoti du tiesiniai bėgančiosios bangos architektūros stiprintuvai. Abustiprintuvai yra identiškos geometrijos, tačiau vieno stiprintuvo užtūros aukštadažnės apkrovos (angl. termination) grandynas buvo integruotas į lustą, o kito – prijungiama prie lusto ant testinės spausdintinės plokštės. Matavimo rezultatai atskleidė, kad stiprintuvo su integruota aukštadažne apkrova stiprinimo S_{21} koeficientas yra stabilesnis veikimo dažnių juostoje (didžiausias nuokrypis nuo maksimalios vertės siekė 4 dB, lyginant su 6 dB kai apkrova buvo lusto išorėje). Toks rezultatas yra paaiškinamas tuo, kad laidininkas, jungiantis patį lustą su pakuotės korpusu, išderina 50 Ω banginės varžos mikrojuostelinę liniją, kuri suformuota stiprintuvo įėjime. Abiejų ištirtų bėgančiosios bangos stiprintuvų veikimo dažnių juosta yra apie 10 GHz, tačiau išmatuotas efektyvumas yra tik 16 %.



(a) (b)

S3.1 pav. Pagamintų integrinių grandynų mikrofotografinės nuotraukos: (a) kalsikinių ir (b) bėgančiosios bangos belaidžio ryšio galios stiprintuvų, taikant *IBM* 0,13 µm KMOP technologiją,

Dėl savo siauros veikimo dažnių juostos klasikinės architektūros GS neužtikrina 5G belaidžio ryšio reikalavimų. Nors bėgančiosios bangos GS praleidžiamųjų dažnių juosta viršija vieną oktavą, tačiau jų efektyvumas yra tik 15–20 %. Todėl, dėl prasto efektyvumo, bėgančiosios bangos galios stiprintuvai taip pat netinka ateities vidutinių dažnių 5G belaidžio ryšio įtaisams kurti. Tuo tarpu Doherty galios stiprintuvų architektūra pasižymi atgalinės galios (angl. back-off power) parametru, kuris nusako, kad tam tikrame įėjimo signalo galios diapazone stiprintuvo efektyvumas išlieka artimas įsisotinusio stiprintuvo efektyvumui.

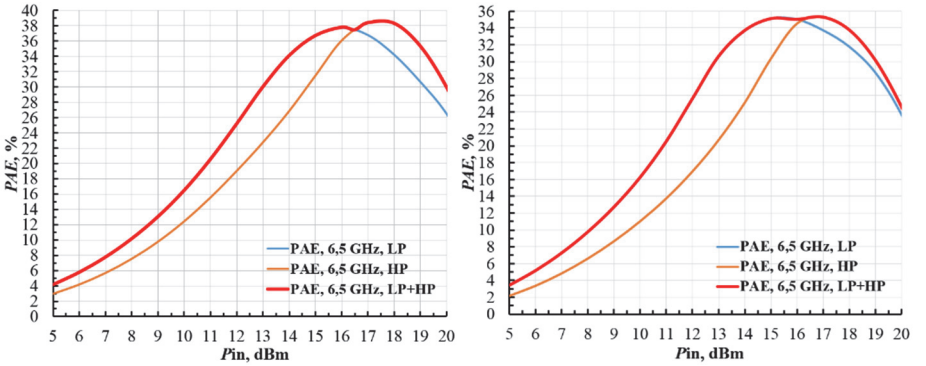
Šios architektūros GS gali būti įgyvendinami viename luste arba naudojant diskrečius komponentus, bei taikant paskirstytųjų ir sutelktųjų parametrų suderinimo grandynų elementus. Be to Doherty GS gali būti taikomos ir linearizavimo metodikos, o jų struktūros neriboja tarpinio dažnio (angl. intermediate frequency) juostos. Dėl išvardintų priežasčių, pasirinkta Doherty GS skirtų 5G belaidžio ryšio tinklams tyrimo kryptis. Kadangi 5G tinklai, lyginant su 4G ir ankstesės kartos tinklais, numato galimybę naudoti nelicencijuotas dažnių juostas bendros paskirties tinkluose. Tai yra nauja koncepcija, kurą įveda 3GPP standartas, kadangi iki šiol buvo naudojami tik uždari licencijuoti dažnių ruožai. To pasėkoje, nelicencijuoti dažnių ruožai Europoje ir JAV įtraukiami į naujojo radijo NR (angl. new radio) grupę, kuri suriša jau esamas technologijas į NR/NR, NR/LTE ir NR/*Wi-Fi* (Qualcomm Technologies Inc., 2017). Tokiu būdu, šioje disertacijoje, tiriant Doherty architektūros stiprintuvus, susitelkta ties nelicencijuotos 5,9–7,1 GHz vidutinių dažnių 5G juostos. Siekiant ištirti Doherty GS buvo suprojektuoti dviejų skirtingų architektūrų stiprintuvai: su klasikiniu ir su supaprastintu išėjimo impedansų inverteriu. Projektavimui buvo panaudotos *TSMC* 0,18 µm KMOP gamybos technologijų bibliotekos. Abiejų suprojektuotų Doherty GS suminės efektyvumo charakteristikos pateiktos S3.2 paveiksle, o keliami reikalavimai ir rezultatų suvestinė pateikti S3.1 lentelėje.

S3.1 lentelė. Klasikinio ir supaprastinto Doherty galios stiprintuvų palyginimas

Parametras	Specifikacija	Klasikinis Doherty GS	Supaprastintas Doherty GS
Veikimo dažnis	6,5 GHz		
Dažnių ruožas	5,9–7,1 GHz	6,2–6,8 GHz	
Juostos plotis	≥150 MHz	600 MHz	
Išėjimo galia	15–24 dBm	21 dBm	20 dBm
Galios stiprinimas	5–10 dB	6–8 dB	5–7 dB
Stabilumas	Besąlygiškai stabilus		
Atgalinė galia	3–6 dB	3 dB	
Efektyvumas	25–35 % prie atgalinės galios	28 % prie atgalinės galios; maksimali 38 % vertė	26 % prie atgalinės galios; maksimali 35 % vertė
Z_L/Z_S	50 Ω		
Užimamas plotas	<1 mm^2	0,722 mm^2	0,639 mm^2
Technologija	*TSMC* 0,18 µm KMOP		

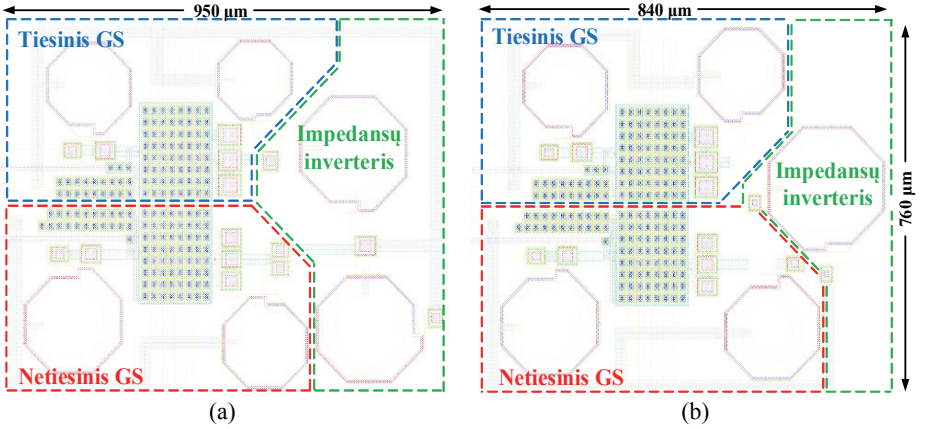
S3.2 paveiksle pateikti stiprintuvo efektyvumo modeliavimo rezultatai esant 6,5 GHz centriniam dažniui. Supaprastinto ir klasikinio Doherty architektūros GS efektyvumo charakteristikos sudarytos iš dviejų šio stiprintuvo veikimo režimų efektyvumo charakteristikų sumos. Suprojektuoto ir ištirto klasikinio Doherty stiprintuvo, kurio užimamas plotas yra 0,722 mm^2, efektyvumas 3 dB atgalinės galios ruože viršija 28 %, o

didžiausias efektyvumas esant stiprintuvo įsisotinimui yra lygus 38 %. Suprojektuoto ir ištirto supaprastinto Doherty GS, kurio užimamas plotas yra 0,639 mm^2, efektyvumas 3 dB atgalinės galios ruože viršija 26 %, o didžiausias efektyvumas esant stiprintuvo įsisotinimui yra lygus 36 %. Nepaisant to, kad supaprastintos konfigūracijos Doherty GS efektyvumas yra 2 % mažesnis negu klasikinės konfigūracijos, išlaikomas šios architektūros pagrindinis privalumas (atgalinės galios ruožas), esant 12 % mažesniam užimamam lusto plotui.



S3.2 pav. Belaidžio ryšio galios stiprintuvų efektyvumo charakteristikos prie 6,5 GHz dažnio *TSMC* 0,18 µm KMOP technologijoje: (a) klasikinė ir (b) supaprastinto inverterio Doherty architektūra

S3.3 paveiksle pateiktos klasikinio ir supaprastinto Doherty galios stiprintuvų topologijos. Suprojektuotų stiprintuvų tranzistorių geometriniai matmenys yra identiški, tačiau skiriasi išėjimo impedansų inverterio konfigūracija.



S3.3 pav. Pasiūlytų belaidžio ryšio galios stiprintuvų topologiniai vaizdai *TSMC* 0,18 µm KMOP technologijoje: (a) klasikinis ir (b) supaprastinto inverterio Doherty architektūros stiprintuvas

Doherty galios stiprintuvo su supaprastintu impedansų inverteriu užimamas plotas yra apie 12 % mažesnis lyginant su klasikiniu Doherty stiprintuvu.Tokiu būdu Doherty galios stiprintuvas su supaprastintu išėjimo impedansų inverteriu gali būti naudojamas naujos kartos vidutinių dažnių 5G belaidžio ryšio didelės integracijos daugiastandarčiuose siųstuvų ir siųstuvų-imtuvų integriniuose grandynuose.

Bendrosios išvados

1. Pasiūlytas kokybinis ir kiekybinis žemadažnio signalo gaubtinės sekimo, fazuojančio, bėgančiosios bangos ir Doherty galios stiprintuvų architektūrų įvertinimas, leidžiantis nustatyti skirtingų gamybos technologijų galios stiprintuvų pritaikomumą naujos kartos tiek žemų, tiek vidutinių, tiek auštų dažnių juostų 5G belaidžio ryšio siųstuvų ir siųstuvų-imtuvų kūrime.
2. Taikant *IBM (GlobalFoundries)* 0,13 μm giliai submikroninę KMOP gamybos technologiją, suprojektuotos ir eksperimentiškai ištirtos klasikinės tiesinės bei bėgančiosios bangos galios stiprintuvų architektūros vidutinių dažnių 5G juostos ribose (ties 2,5 GHz ir ties 6,5 GHz), kurių maksimaliai pasiekiamas efektyvumas yra iki 25 %, veikiant prie skirtingų įėjimo signalo galių ir atitinkamai pasižymi didžiausiu suderinimo juostos pločiu iki 400 MHz bei daugiau negu viena oktava.
3. Taikant giliai submikroninę *TSMC* 0,18 μm KMOP technologiją, suprojektuoti ir eksperimentiškai ištirti du, klasikinės Doherty ir su supaprastintu išėjimo impedansų inverteriu, architektūros galios stiprintuvai, užtikrinantys virš 25 % efektyvumą, esant 3 dB atgalinei galiai, ir didžiausią 38 % efektyvumą ties 6,5 GHz centriniu dažniu, o panaudojus supaprastintą inverterį net 12 % sumažinamas ir užimamas lusto plotas.
4. Atsižvelgus į tai, kad iki šiol pasiūlytos impedansų suderinimo grandynų apskaičiavimo metodikos įvertina tik komponentų ekvivalentinę nuosekliąją varžą, pasiūlytas naujas matematinis modelis ir ISGS algoritmas, įvertinantis sutelktųjų parametrų komponentų parazitinius parametrus, sumažinantis S_{11} charakteristikos minimumo didžiausią nuokrypį nuo ieškomo dažnio iki 1–7 % taikant 0402 pakuotės komponentus su 10 % neapibrėžtimi.
5. Siekiant sumažinti galios stiprintuvams skirtų grandynų projektavimo trukmę bei gamybos kaštus, siūloma pirmiausia nustatyti jautriausią komponentą suderinimo charakteristikos S_{11} poslinkiui dažnių ašyje, ir naudoti mažesnės iki 5 % neapibrėžties komponentą, o kitiems suderinimo grandyno komponentams gali būti panaudoti ir didesnės, IEC/EN 60062 standarte reglamentuojamos, neapibrėžties komponentai.
6. Pasiūlyti nauji impedansų suderinimo grandynų algoritmas ir matematinis modelis, įgyvendinti *IMNS Toolbox* įskiepio į profesionalią integrinių grandynų projektavimo aplinką *Cadence Virtuoso* pavidalu, sumažinant modeliavimo ir matavimų iteracijų skaičių iki 1 iteracijos 1 MHz – 1 GHz dažnių ruože ir iki 1–3 iteracijų kai ruožas yra 1–3 GHz.

Annexes[1]

Annex A. Declaration of Academic Integrity

Annex B. The Coauthors' Agreements to Present Publication Material in the Dissertation

Annex C. Copies of Scientific Publications by the Author on the Topic of the Dissertation

[1]The annexes are supplied in the enclosed compact disc

Aleksandr VASJANOV

MID-BAND 5G WIRELESS NETWORK POWER AMPLIFIER RESEARCH

Doctoral Dissertation

Technological Sciences,
Electrical and Electronic Engineering (T 001)

VIDUTINIŲ DAŽNIŲ 5G BELAIDŽIŲ TINKLŲ GALIOS STIPRINTUVŲ TYRIMAS

Daktaro disertacija

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